11 AC/DC Grid Interface Based on the Three-Phase Voltage Source Converter

11.1 PARTICULARITIES, CONTROL OBJECTIVES, AND ACTIVE POWER CONTROL

As energy is mostly transported on AC lines, electronic circuits able to convert AC to DC voltages have been the first application ever for power semiconductor devices [22–27]. The diode rectifier is the simplest power converter grid interface (Figure 11.1). At larger power levels, energy is transported and distributed within three-phase systems, and conversion from three-phase AC to DC voltage is used. All design aspects of diode rectifiers are thoroughly presented in university textbooks for power electronics and will not be reproduced here. However, Table 11.1 reviews the possible diode rectifier solutions and the appropriate factors for the waveform quality.

It is important to note that the high harmonic content of the grid currents may not be in accordance with the modern standards for power quality for certain power levels. Chapter 1 has shown some of the main requirements expected from power converters in different countries. It is easy to observe that above a certain level of the grid current, this class of topologies does not satisfy power quality requirements.

The second obvious disadvantage of this topology is the lack of control for the output voltage. Historically, this drawback was first tackled with thyristor (SCRs)-based converters (Figure 11.2). Their operation assumes a phase control and an output voltage lower than the diode rectifier's output voltage. The waveforms corresponding to the operation of this power stage outline the low power factor and large reactive power circulated in the system.

The advent of power semiconductor devices with turn-off capability has improved the power quality factors for the grid currents. The first use of gate-turn-off thyristor (GTO) devices within the diode or SCR-rectifier topologies has opened a new class of power converters. Examples of pioneering solutions are shown in Figure 11.3.

The output voltage results in a train of pulses characterized by a DC component and an HF-switching component. The grid current equals the algebraic sum of the currents through two devices and follows the pulse control strategy. This allows total harmonic distortion (THD) or, generally, the harmonic content of the grid current to improve. Given the large inductance in the load, a pulse is seen in the line current during each interval when a voltage pulse is generated on the load (Figure 11.4).

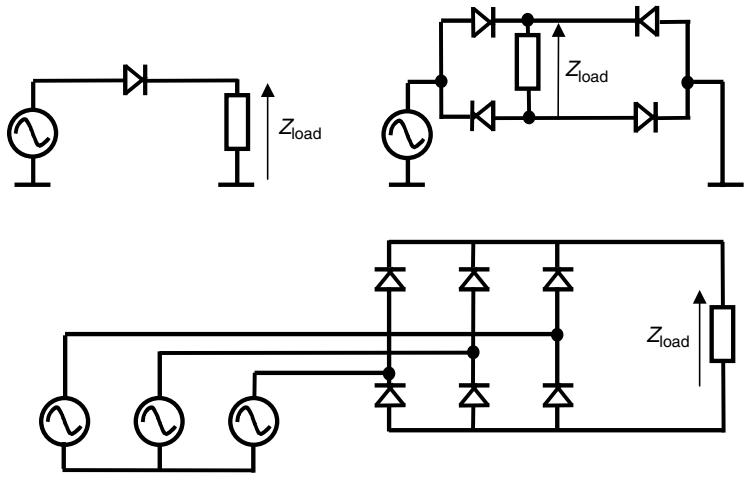


FIGURE 11.1 Different topologies of diode rectifiers.

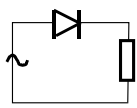
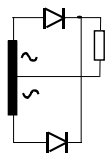
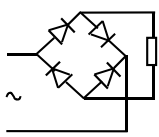
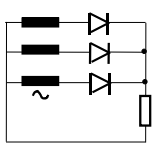
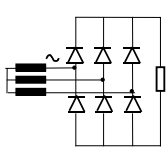
If the number of pulses is small, a control strategy able to eliminate low harmonics (5th, 7th, 11th, 13th, and so on) of the current waveform is employed. Details of designing a pulse width modulation (PWM) controller suitable for such an operation are presented in Chapter 4. If the power semiconductor devices allow a higher switching frequency, a sinusoidal PWM algorithm may be considered. Two switches are controlled at a given moment and the pulse width is derived with a sinusoidal law.

All these circuits switch current through the grid lines. They introduce a line inductance in the path of the switch current, creating overvoltage at switching. To overcome this, snubber capacitors are needed across the power semiconductor devices (Chapters 2 and 3).

All the previously introduced power converters ensure energy conversion towards a load with a large inductance. This is the case when a DC machine drive or a DC magnet supply is used. However, a large group of applications require supply of the load with a constant DC voltage. This includes also the case of a grid interface for AC machine drives in which the DC circuit is dominated by a very large capacitor. Details about rating the DC bus and the importance of the proper value for a specific AC machine drive application are discussed in Chapter 4. We present here the details of the grid interface.

The simplest circuit able to create voltage on the DC intermediary circuit is based on a diode rectifier. As both the grid and the DC bus are voltage sources, an inductance should be used to take over instantaneously the differences between these two voltage sources. Different solutions use the inductance on the DC side, on the grid side, or on both sides. When the inductance is on the DC side, the circuit operation is identical to the previous diode rectifier with a large inductive load. The rectifier bridge produces an output voltage following the envelope of the grid voltages, and the inductance acts as a filter to produce the constant DC bus voltage (Figure 11.5).

TABLE 11.1
Performance of Different Diode Rectification Schemes without Output Capacitor Filter

Topology	Number of diodes	Semiconductor ratings [V/I]	Output average voltage
Single-phase			
	1	V_{in}, I_{pk}	$V_{d0} = V_{ph}\frac{\sqrt{2}}{\pi}$
	2	V_{in}, I_{pk}	$V_{d0} = V_{ph} = \frac{2\sqrt{2}}{\pi}$
	4	$V_{in/2}$, I_{pk}	$V_{d0} = V_{ph} = \frac{2\sqrt{2}}{\pi}$
Three-phase			
	3	VLL, I_{pk}	$V_{d0} = \sqrt{2}V_{ph}\frac{3\sqrt{3}}{2\pi}$
	6	VLL, I_{pk}	$V_{d0} = 2\sqrt{2}V_2\frac{3\sqrt{3}}{2\pi}$

When the inductance is on the AC side, the diodes have a shorter conduction angle depending on the actual voltage of the DC bus capacitor. Figure 11.6 shows the topology and the main waveforms for this AC/DC converter. When the difference between two line voltages is larger than the DC bus voltage, a pair of diodes turns on and the capacitor voltage follows the grid line-to-line voltage (VLL). This interval corresponds to charging energy within the DC bus capacitor. When

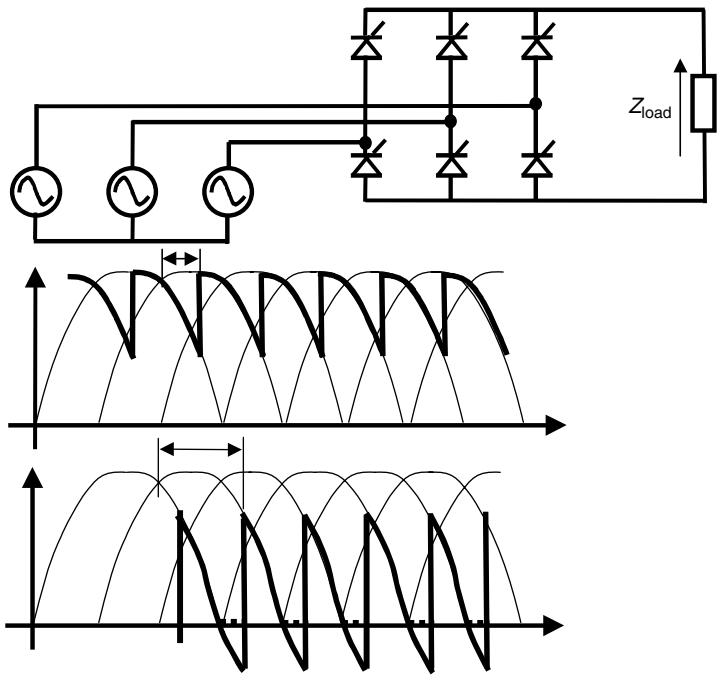


FIGURE 11.2 SCR-based bridge converter and output voltage waveforms for different phase angle controls.

the DC bus voltage reaches the level of VLL, the diodes turn-off and the load is supplied solely from the capacitor bus. During the short conduction time interval of the diodes, the charging current is quite high, as it is produced across a small grid inductance from a large voltage difference. Moreover, the charging current at the start-up is very high until the bus voltage reaches the envelope of the grid voltages.

The output of the rectifier bridge represents a quasi-constant DC voltage with a level dictated by the grid peak voltage. The level of the DC bus voltage depends slightly on the load. If there is no load, the DC voltage follows exactly the peak of VLLs. The higher the load current, the larger the ripple of the voltage across the capacitor produced by subsequent charge–discharge events. The maximum ripple corresponds to the diode rectification waveform of VLLs.

11.2 PWM IN THE CONTROL SYSTEM

11.2.1 Single-Switch Applications

As previously shown, there is no control of the level of the DC bus voltage, and the grid currents are formed by pulses of current. A simple solution would consist of a buck or boost converter following up the DC capacitor (Figure 11.7).

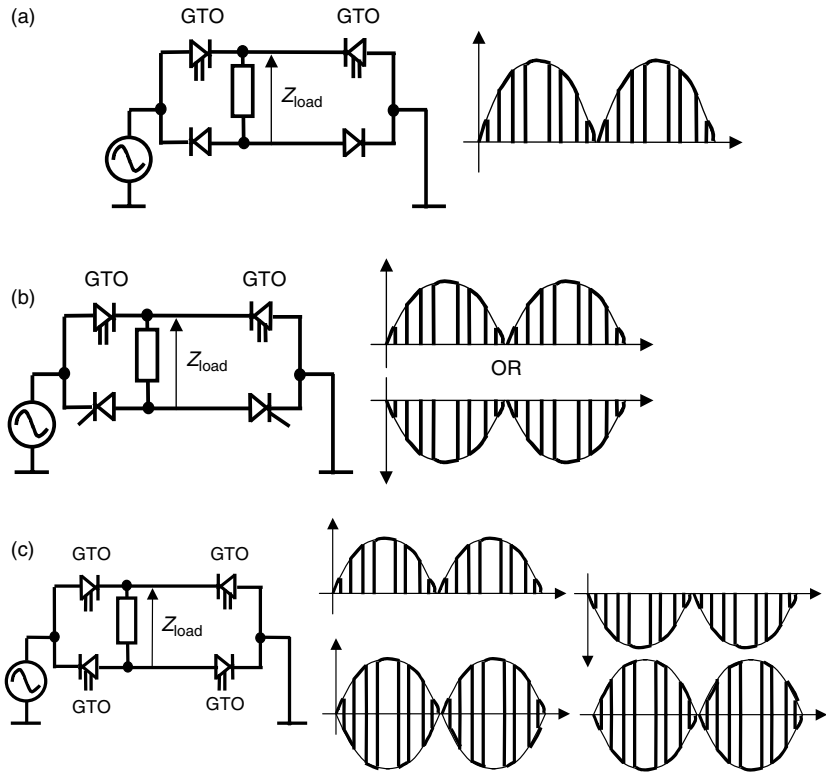


FIGURE 11.3 Use of GTO devices within single-phase grid interfaces.

There is a double DC stage within these converter topologies and this implies large filter DC capacitors. A closer analysis shows that the output voltage can be achieved after a multiplication of the switching functions corresponding to the two power-converter stages. This is equivalent to considering a single-capacitor

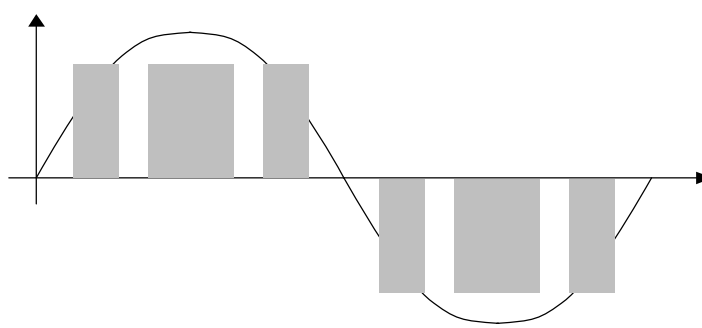


FIGURE 11.4 Pulses within the grid current.

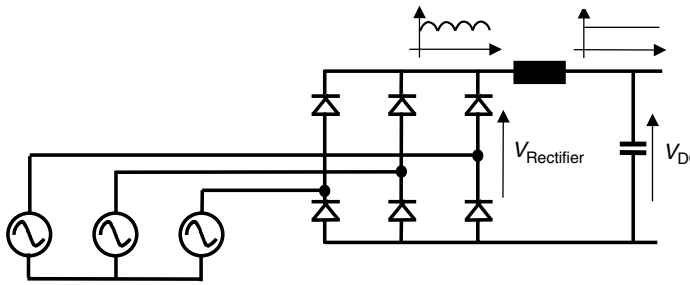


FIGURE 11.5 Diode rectifier with an inductive filter on the DC side.

filter at the output of the second power converter. In other words, it is possible to use the rectified voltage directly at the input of the buck or boost converter.

Moreover, it is desirable that the grid current be as close as possible to a sinusoidal waveform with reduced harmonics. The operation of the boost converter ensures this behavior of a continuous input current, with a waveform close to a given reference. This is because the inductor appears on the grid side and the inductor current is not chopped during operation. The resulting possible topologies are shown in Figure 11.8. Among these, the circuit with grid-side inductance is preferred because of the AC character of the current through inductors. The second major advantage of this topology consists of the inherent high power factor of the grid current.

Rectifying the AC input using a diode rectifier and chopping it at a high frequency to achieve voltage control has the advantages of simplicity, performance, and reliability. A diode rectifier cascaded with a PWM boost chopper is analyzed in [1–7]. In the first solution [1], the boost inductance is present in the grid side as phase inductance (Figure 11.8a). The analysis and design of this converter is further described in the work of Kolar et al. [2,3].

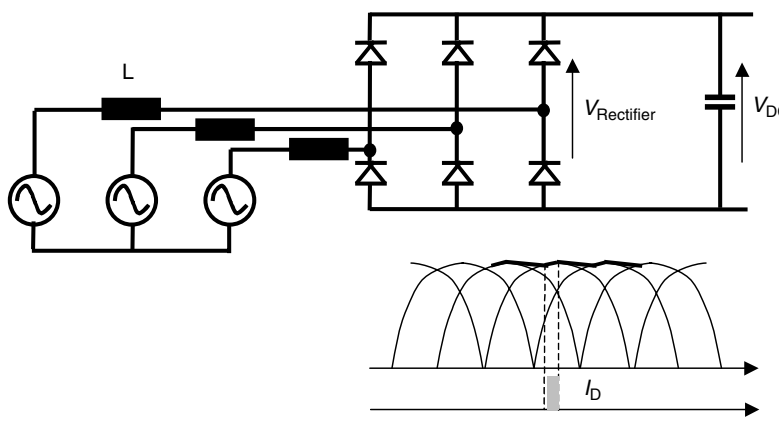


FIGURE 11.6 Diode rectifier with an inductive filter on the DC side.

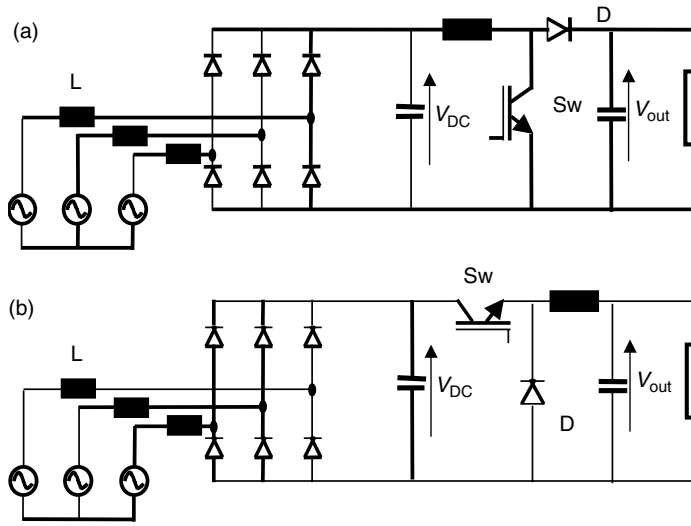


FIGURE 11.7 DC/DC converters following up a diode rectifier stage.

The step-up (boost) converter operates at constant frequency in the discontinuous mode. This mode has some disadvantages:

- Higher voltage/current stress
- Electro-magnetic inference propagation

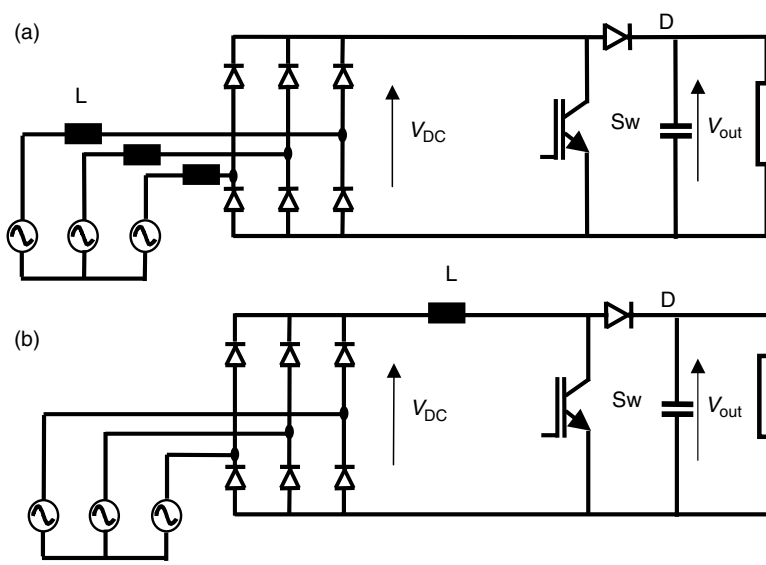


FIGURE 11.8 Three-phase single-switch boost converter.

Advantages consist of

- High input power factor
- Reduced power loss through zero-current switching
- The absence of reverse recovery problem in the diodes
- The possibility of single control loop to control output power and voltage

Using this approach in high-power applications operated with low switching frequency and producing a low output voltage leads to a lower grid power factor and a current THD greater than 5%. One solution consists of injecting a harmonic content within the control of the switch in order to compensate for the main current harmonics.

The conventional control of the boost converter grid interface is simple, but the advantages of PWM are not fully utilized yet. It has been shown in the work of Weng and Yuvarajan [6,7] by extensive computer analysis that the input current distortion for a single-phase converter is reduced when employing a PWM with a second harmonic signal injected within the reference. The reference signal for the PWM generation is usually a DC value able to define the output voltage level. By injecting a second-order harmonic synchronized with the grid, the inherent variations of the output voltage and input current with the phase of the grid are reduced (Figure 11.9).

The circuit contains a low-pass grid filter that allows the input voltage to be seen directly at the converter input. The second inductance of the filter (L_b) also acts as a boost inductance for the converter. The switch used in this boost converter can be power MOSFET or insulated gate bipolar transistor (IGBT), depending on the application. When the IGBT "T" is ON, the boost inductances are supplied by phase voltages and energy is stored in their magnetic fields. Depending on the phase of

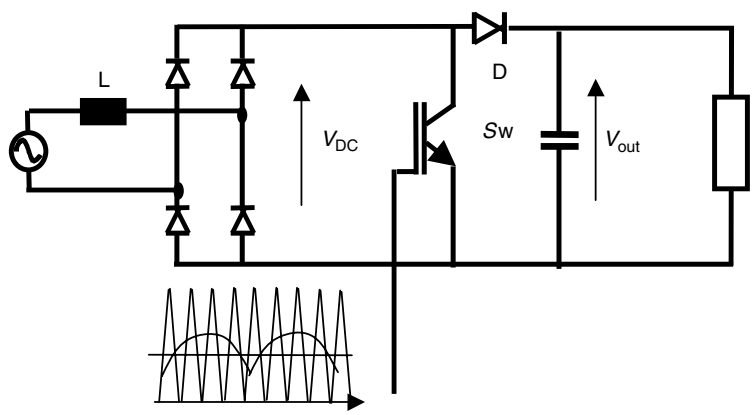


FIGURE 11.9 Injection of the second harmonic within the reference signal of a single-phase boost converter.

the input voltages, three diodes are in conduction at any time. This ON-time interval usually has a constant width and it can modify the output voltage on the basis of the duty ratio. When IGBT is turned-off, the energy stored within the boost inductance is transferred to the output capacitor. As with any boost converter in discontinuous conduction mode, the transfer to the output capacitor is ended when the current vanishes. The duration of this operation (t_{off1}) until the first phase current reaches zero depends on the stored energy and, therefore, on the value of the lowest phase voltage. Observing the phase voltages within a three-phase system defines 12 intervals for analysis, each interval having a different phase voltage with the lowest value. The following discharge interval (t_{off2}) is characterized by the conduction of two diodes only.

Figure 11.10 shows PSPICE simulation results, for example, for the current waveforms given for the case $v_R > 0$, $v_s < 0$, $v_T < 0$. The first current to reach zero is on phase T. Maximum values of the current are denoted by $I_{m,r(s,t)}$ and current levels in the first two phases when the third-phase current vanishes are denoted by $I_{o,r(s)}$. The second waveform always represents voltage shape at the diode rectifier input on the corresponding phase.

From this generic operation of the power stage, different PWM control solutions are considered in the work of Kolar et al. [3].

- Constant ON time and constant switching frequency.
- Variable switching frequency depending on IGBT's turn-on immediately after the end of the inductance's discharge interval, with operation at the border of discontinuous conduction mode.
- Maintaining a constant DC power flow on the DC side by a highly dynamic output voltage control. This solution requires a very large bandwidth of the system.

Understanding all aspects of the operation of the power converter shown in Figure 11.11 and the principles of the harmonic injection, as explained in Figure 11.9, for the single-phase converter allows the development of a special PWM algorithm with performance improvements. The duration of the first time interval after the IGBT's turn-off depends on the instantaneous value of the lowest phase voltage, and this can be compensated for by an appropriate modulation of the reference signal for the PWM control. If the constant duty cycle of the conventional operation is denoted by D_0, the new reference signal for the PWM control is given by:

$$D(t) = D_0(1 + f(t)) \tag{11.1}$$

The injected harmonics are included in the $f(t)$ function. The ON time of the switch is defined as:

$$t_{on} = (D_0 + f(t))T_s = DT_s \tag{11.2}$$

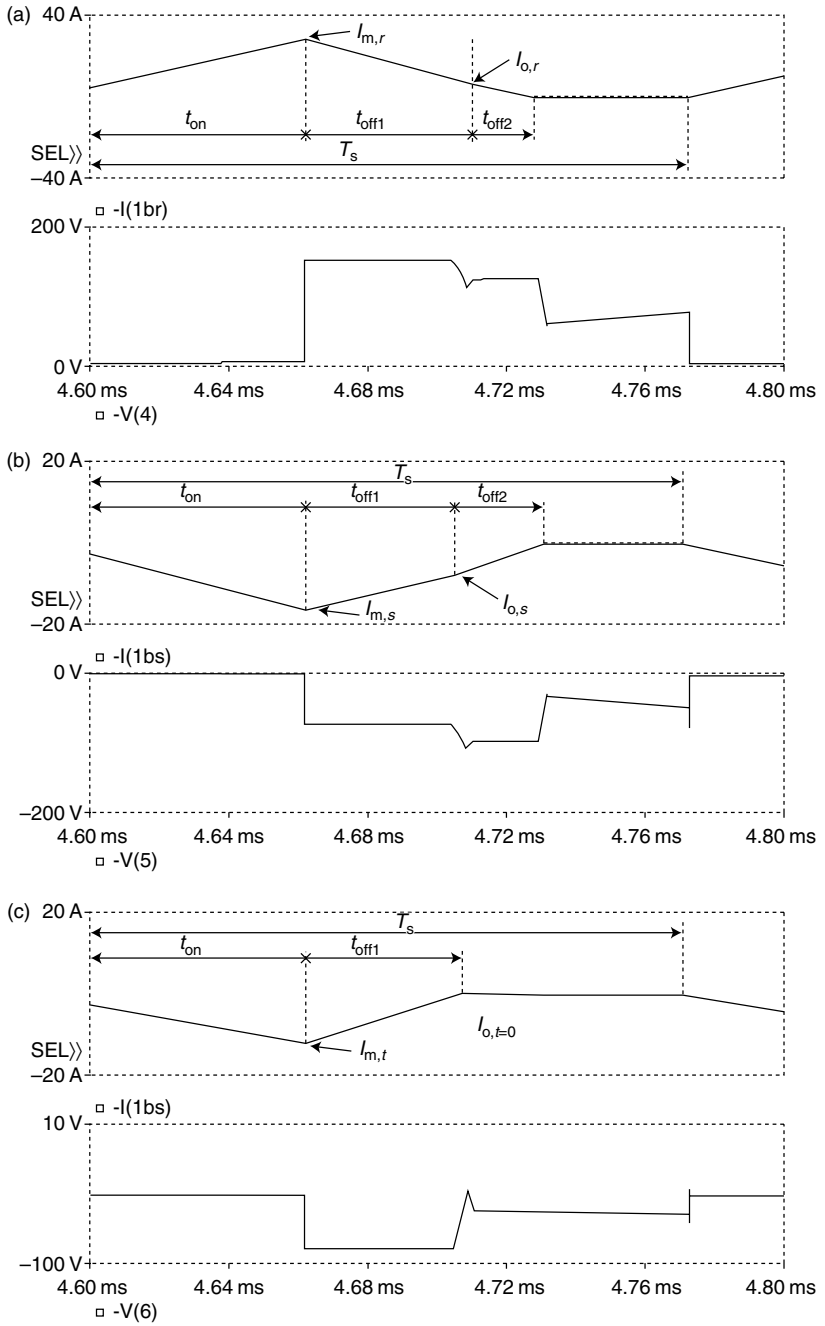


FIGURE 11.10 Shapes of the converter input currents and voltages for (a) phase R, (b) phase S, and (c) phase T. (From Neacsu DO, Yao Z, and Rajagopalan V, IEEE PESC Conference 1996, Baveno, Italy, 1986, 24–27, pp. 727–727, IEEE Paper 0-7803-3500-7/96. (With permission.)

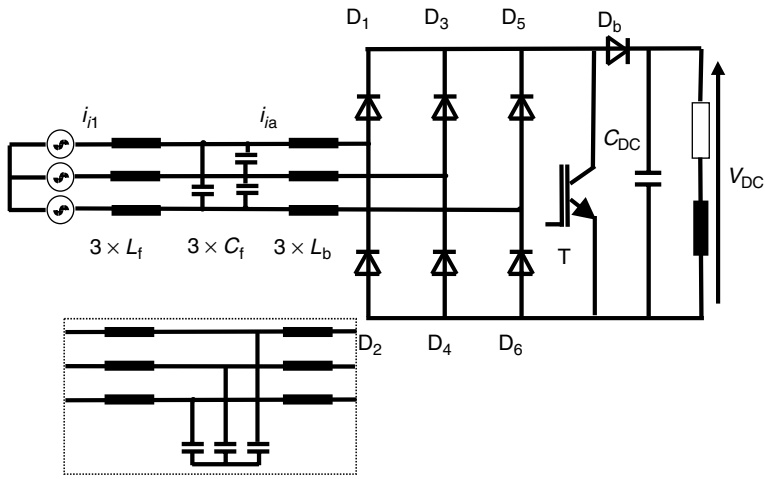


FIGURE 11.11 Basic single-switch three-phase boost converter.

A qualitative analysis of the converter operation reveals the important six-order harmonic as a component of the $f(t)$ function. There are different methods to define the exact or mathematical form of this function. Many solutions are based on repetitive simulation or experimental analysis. In what follows, theoretically derived expressions of phase currents are solved for a problem of optimality and the appropriate computer based implementation is discussed.

However, this optimal PWM improves the harmonic performance at the input of the power converter stage and the actual filter also influences the grid harmonic performance.

Let us derive the mathematical expressions for currents through the boost inductance [7] assuming:

- Symmetrical three-phase system with no neutral components.
- Neglect of losses in the converter.
- Same value of the boost inductors in all three phases.
- All currents are positive when entering the power stage and negative when they flow into the grid.
- High switching frequency allowing an approximation of constant grid voltages over the sampling period and a linear variation of the inductor current over t_{on} and t_{off1}.
- The input filter effect to evaluate grid currents by averaging the converter input currents in each sampling interval.
- The symmetry of a three-phase system to reduce the analysis for a 30° interval (symmetrical evolution on the next 30° is achieved and evolution on the other 60° sectors can be defined by changing the phase sequence.
- The interval shown in Figure 11.10 is considered.

A mathematical form for the phase voltages is shown as:

$$\begin{aligned} v_{\mathrm{R}} &= V\cos(\omega t) \\ v_{\mathrm{S}} &= V\cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_{\mathrm{T}} &= V\cos\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{11.3}$$

We develop the analysis for the 30° interval before the peak of the grid voltage on phase R.

The average relationship for the input current on phase R yields (Figure 11.10):

$$\frac{t_{\mathrm{on}} I_{\mathrm{m},r}}{2} + \frac{t_{\mathrm{off}1}(I_{\mathrm{m},r} + I_{\mathrm{o},r})}{2} + \frac{t_{\mathrm{off}2} I_{\mathrm{o},r}}{2} = I_{\mathrm{R,av}} T_s \tag{11.4}$$

Now, let us define mathematically each time interval. The ON time has already been defined by Equation (11.2) and the first discharge interval depends on the instantaneous value of the voltage on the last phase.

$$t_{\mathrm{off}1} = \frac{t_{\mathrm{on}} V_1}{V_2 - V_1} \Longrightarrow t_{\mathrm{off}1} = \frac{v_{\mathrm{T}}}{-(1/3)V_{\mathrm{DC}} - v_{\mathrm{T}}} t_{\mathrm{on}} \Longrightarrow t_{\mathrm{off}1} = \frac{-v_{\mathrm{T}}}{(1/3)V_{\mathrm{DC}} + v_{\mathrm{T}}} t_{\mathrm{on}} \tag{11.5}$$

The bend-point value of the current on phase R when the current on phase T vanishes yields:

$$I_{\mathrm{o},r} = I_{\mathrm{m},r} - \Delta I = \frac{t_{\mathrm{on}} v_{\mathrm{R}}}{L} - \frac{t_{\mathrm{off}1}[(2/3)(V_{\mathrm{DC}} - v_{\mathrm{R}})]}{L} \tag{11.6}$$

$$I_{\mathrm{o},r} = \frac{t_{\mathrm{on}} v_{\mathrm{R}}}{L} - \left[\frac{-v_{\mathrm{T}}}{V_{\mathrm{dc}} + 3v_{\mathrm{T}}} t_{\mathrm{on}}\right]\left[\frac{2V_{\mathrm{DC}} - 3v_{\mathrm{R}}}{L}\right] \tag{11.7}$$

$$I_{\mathrm{o},r} = \frac{t_{\mathrm{on}}}{L} V_{\mathrm{DC}} \frac{v_{\mathrm{R}} + 2v_{\mathrm{T}}}{V_{\mathrm{DC}} + 3v_{\mathrm{T}}} \tag{11.8}$$

During the first discharge interval, D_1, D_4, and D_6 were in conduction. The second discharge interval for phase R ($t_{\mathrm{off}2}$ in Figure 11.10) is characterized by the conduction of D_1 and D_4 only.

$$I_{\mathrm{o},r} = \frac{t_{\mathrm{off}2}}{L}\frac{1}{2}[V_{\mathrm{DC}} - v_{\mathrm{R}} + v_{\mathrm{S}}] \tag{11.9}$$

It yields:

$$t_{\text{off2}} = 2V_{\text{DC}}t_{\text{on}}\,\frac{v_{\text{R}} + 2v_{\text{T}}}{V_{\text{DC}} + 3v_{\text{T}}}\,\frac{1}{V_{\text{DC}} - v_{\text{R}} + v_{\text{S}}} \tag{11.10}$$

Taking into account all these equations in the current average relationship yields:

$$\begin{aligned} I_{\text{R,av}} = \frac{D^2T_s}{2L}\Bigg\{ & v_{\text{R}} - \frac{3v_{\text{T}}}{[V_{\text{DC}} + 3v_{\text{T}}]^2}[v_{\text{R}}(V_{\text{DC}} + 3v_{\text{T}}) + V_{\text{DC}}(v_{\text{R}} + 2v_{\text{T}})] \\ & + \left[V_{\text{DC}}\,\frac{v_{\text{R}} + 2v_{\text{T}}}{V_{\text{DC}} + 3v_{\text{T}}}\right]^2\left[\frac{2}{V_{\text{DC}} + v_{\text{S}} - v_{\text{R}}}\right]\Bigg\} \end{aligned} \tag{11.11}$$

Currents on the other two phases are given without demonstration, but they can be calculated as an exercise.

$$I_{\text{T,av}} = \frac{D^2T_s}{2L}\,\frac{v_{\text{T}}}{V_{\text{DC}} + 3v_{\text{T}}}\,V_{\text{DC}} \tag{11.12}$$

$$\begin{aligned} I_{\text{S,av}} = \frac{D^2T_s}{2L}\Bigg\{ & \left[v_{\text{S}} - \frac{3v_{\text{T}}}{[V_{\text{DC}} + 3v_{\text{T}}]^2}[v_{\text{S}}(V_{\text{DC}} + 3v_{\text{T}}) - V_{\text{DC}}(v_{\text{R}} + 2v_{\text{T}})]\right] \\ & - \left[V_{\text{DC}}\,\frac{v_{\text{S}} - v_{\text{T}}}{V_{\text{DC}} + 3v_{\text{T}}}\right]^2\left[\frac{2}{V_{\text{DC}} + v_{\text{S}} - v_{\text{R}}}\right]\Bigg\} \end{aligned} \tag{11.13}$$

These expressions are analogous with the results presented in the work of Kolar et al. [2,3], but with an explicit dependence on the circuit voltages and are very suitable for computer implementation and solving.

The goal for computer optimization is to determine the modulation function $f(t)$, which reduces the input current harmonics. In this respect, the optimization condition is written as the cumulative error from a set of input currents with sinusoidal waveforms and synchronized with the grid voltages. In a real implementation, the root mean square value of these reference currents is calculated from the power-transfer condition through the power converter.

$$\min\lfloor(I_{\text{R,av}} - i_{\text{R}})^2 + (I_{\text{S,av}} - i_{\text{S}})^2 + (I_{\text{T,av}} - i_{\text{T}})^2\rfloor \tag{11.14}$$

The first possibility to solve this optimal problem consists of using a mathematical program, such as MathCad. One should solve the constraint (11.14) for each phase angle of the input voltage within a sector of 30° before the peak of the voltage on phase R. Results for different duty cycles are shown in Figure 11.12. As the preliminary understanding of the problem indicated that a sixth-order harmonic may be the optimal injected signal, the appropriate modulation signal for

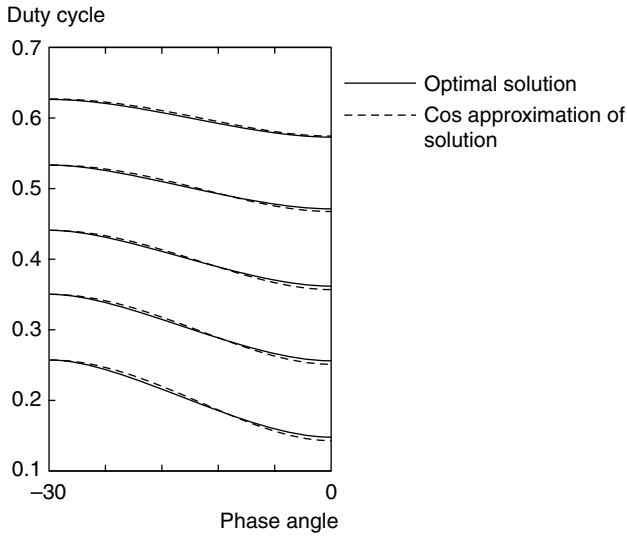


FIGURE 11.12 Results for the duty cycle modulations for the same phase as in Equation (11.3). (From Neacsu DO, Yao Z, and Rajagopalan V, IEEE PESC Conference 1996, Baveno, Italy, June 1996, 24–27, pp. 727–727, IEEE Paper 0-7803-3500-7/96. With permission.)

a cosine approximation is also shown. This approximation is very important for the actual implementation of the controller.

Notice a linear dependence of the amplitude of the cosine modulation waveform on the switch duty cycle. The amplitude is given by this linear dependence, whereas the phase variation is achieved with a phase locked-loop (PLL)-based circuit for synchronization with input line voltages. The modulation wave thus obtained is used with a classical PWM integrated circuit (IC) to control the switch.

Taking into account the power conservation principle can help demonstrate that each $2n$th harmonic in the power converter's output voltage is related to the input current harmonics of orders $2n + 1$ and $2n - 1$ (output constant load, input symmetrical system). For instance, an action against the 6th harmonic in the output would also minimize the effect of both 5th and 7th harmonics in the input current.

Injection of a harmonic signal within the reference for the PWM control is able to correct the ideal low-frequency shape of the input current. Figure 11.13 presents theoretical low-frequency components for the cases with and without harmonic injection.

The actual input current harmonics are also influenced by the input filter. One of the negative effects of the input filter that adds up to delays in the control system and the effect of the sampling interval is the phase shift between the input voltage and current. To compensate for this phase delay, a small phase shift should be considered within the harmonic injection reference.

Figure 11.14 and Figure 11.15 show harmonic results when this solution is considered within a power converter-based grid interface. The THD of the input current

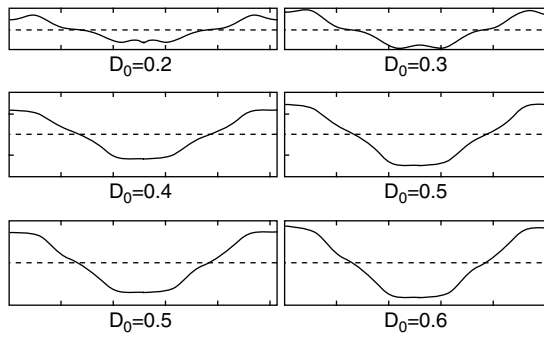


FIGURE 11.13 Input current theoretical waveforms: solid line, without modulation; dashed line, with modulation. (From Neacsu DO, Yao Z, and Rajagopalan V, IEEE PESC Conference 1996, Baveno, Italy, June 1996, 24–27, pp. 727–727, IEEE Paper 0-7803-3500-7/96. With permission.)

is still above 5%, but Figure 11.14 does not include the effect of the input filter. The remaining harmonics are at higher frequencies, and they can be removed with a conventional low-pass filter. As the optimal PWM reduces the content in the low frequencies, 5th and 7th harmonics of the input current for the case without harmonic injection and for the case with harmonic injection are shown in Figure 11.15. It can be seen that the cumulative effect of both 5th and 7th harmonics is reduced by this approach: $(\min(V_5^2 + V_7^2))$. For a switching frequency of 5 kHz, the content in low harmonics for the case without optimal modulation is $I_5 = 6.77\%$ and $I_7 = 1.01\%$, whereas the case with optimal PWM leads to $I_5 = 3.84\%$ and

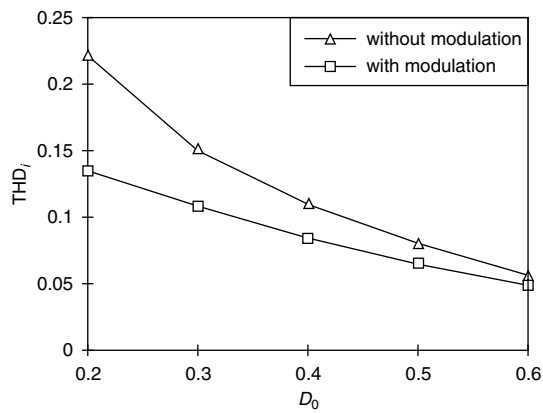


FIGURE 11.14 THD for input current over the switch duty cycle computed with the first 500 harmonics. (From Neacsu DO, Yao Z, and Rajagopalan V. IEEE PESC Conference 1996, Baveno, Italy, June 1996, 24–27, pp. 727–727, IEEE Paper 0-7803-3500-7/96. With permission.)

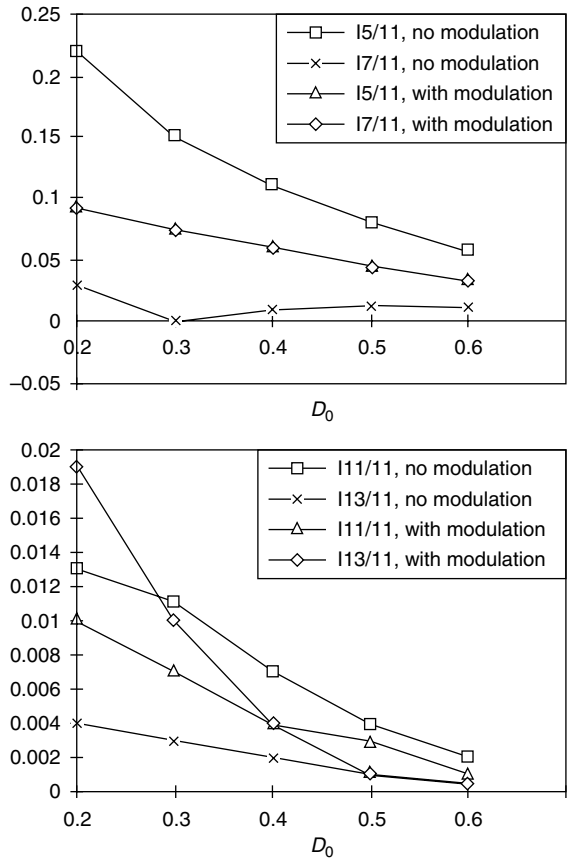


FIGURE 11.15 Low harmonics content of the input currents. (From Neacsu DO, Yao Z, and Rajagopalan V, IEEE PESC Conference 1996, Baveno, Italy, June 1996, 24–27, pp. 727–727, IEEE Paper 0-7803-3500-7/96. With permission.)

$I_7 = 3.83\%$. However, both harmonics are inside the limits imposed by IEC 555-2 ($I_5 = 1.14\,A$ and $I_7 = 0.77\,A$) for the output powers in the kilowatt region. For $D > 0.5$, the content in both harmonics is less than 4% as required by IEEE 519-1992.

The harmonic injection in the PWM reference signal of a single-switch three-phase PWM boost converter has the following advantages:

- Reduced instability risk due to discontinuous conduction mode
- Applicable to the single-switch three-phase boost converter topologies (including the modern resonant ones) with minimal and low-cost modifications of the command circuit
- Implementation with any conventional PWM IC owing to the operation with constant switching frequency

- Reduced requirements for the mains filter and enlarged domain of having input THD current less than 5% and input power factor greater than 95%.

11.2.2 Six-Switch Converters

Many applications require a bidirectional power transfer to the grid, and this implies moving the boost power converter stage closer to the grid without the intermediate stage of diode rectification. Figure 11.16 shows the three-phase six-switch power converter. Chapter 3 introduced this power stage with applications to DC/AC conversion and AC motor drives. The same power converter with a different control is the most important three-phase electronic grid interface.

This topology allows a bidirectional power flow with the control of both the DC bus voltage and the input power factor, although the input currents have low harmonics [15–21]. This ensures a very high performance interface to the grid for different industrial equipment, such as electrical drives or DC load supply. Electrical drives with AC/DC boost bridge converters also benefit from energy savings during braking or acceleration during drive dynamics. Controlling the DC bus voltage allows capacitor discharge into the grid instead of on a dummy brake resistor (Figure 11.16).

Let us develop a mathematical model for the analysis of this power converter starting from the grid electrical circuit. The grid voltages are defined as:

$$\begin{aligned} e_{a0} &= E\sin(\omega t) \\ e_{b0} &= E\sin\left(\omega t - \frac{2\pi}{3}\right) \\ e_{c0} &= E\sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{11.15}$$

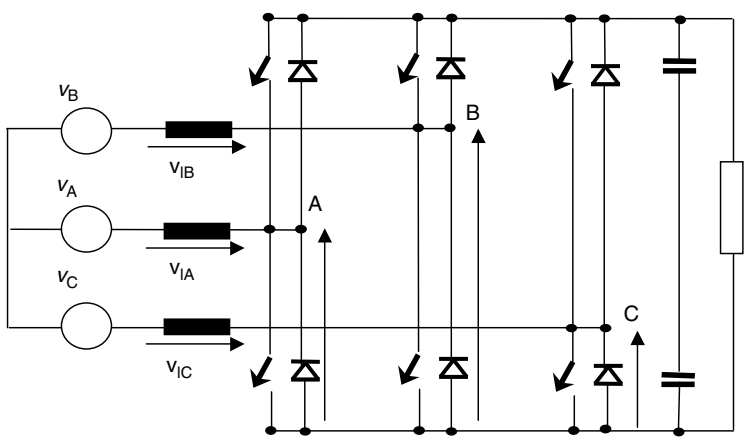


FIGURE 11.16 Three-phase grid interface with six switches.

The voltage equations for each phase can be expressed dependent on each pole voltage from the power converter.

$$\begin{aligned} e_{a0} &= R_r i_{1a} + L_r \frac{di_{1a}}{dt} + v_{a0} \\ e_{b0} &= R_r i_{1b} + L_r \frac{di_{1b}}{dt} + v_{b0} \\ e_{c0} &= R_r i_{1c} + L_r \frac{di_{1c}}{dt} + v_{c0} \end{aligned} \tag{11.16}$$

The first approach to the analysis of this converter was developed with a scalar control of the DC voltage through the modulation index of the PWM references synchronized with the AC grid voltage [8]. The difference between the fundamental of the voltage generated by PWM and the grid voltage is applied to the boost inductance, defining the input currents. Given the inherent phase shift produced by an inductor, the control references should be appropriately shifted and synchronized.

A second approach consisted of the so-called delta control of the power converters, [9] which is an equivalent of the hysteresis control method.

Later on, vectorial methods [3–6] were preferred for control of this power converter [7,10,11]. The vectorial methods for three-phase systems have been presented in Chapter 6 for DC/AC converters and they can be extended to AC/DC conversion. They provide high performance current control in the d–q frame and have the particular advantage of separating the active and reactive power components. As one of the most important requirements for the grid interfaces is the unity or controllable power factor, this features become very important.

The three-phase system of equations from Equation (11.16) can be transformed in an equivalent two-phase system expressed by:

$$\begin{aligned} e_{x0} &= R_r i_{1x} + L_r \frac{di_{1x}}{dt} + v_{x0} \\ e_{y0} &= R_r i_{1y} + L_r \frac{di_{1y}}{dt} + v_{y0} \end{aligned} \tag{11.17}$$

The transformation of these equations into the synchronous reference frame

$$\begin{aligned} v_d &= v_{x0} \cos\theta + v_{y0} \sin\theta \\ v_q &= -v_{x0} \sin\theta + v_{y0} \cos\theta \end{aligned} \tag{11.18}$$

yields the input voltage equations in the synchronous d–q reference frame

$$\begin{aligned} e_d &= R_r i_d + v_d + L_r \frac{di_d}{dt} - \omega L_r i_q \\ e_q &= R_r i_q + v_q + L_r \frac{di_q}{dt} + \omega L_r i_d \end{aligned} \tag{11.19}$$

The grid voltages are expressed by two constant components:

$$\begin{aligned} e_d &= E \\ e_q &= 0 \end{aligned} \tag{11.20}$$

Equation (11.19) and Equation (11.20) demonstrates that the grid current can be decomposed into two components:

- i_q allows the control of the input reactive power.
- i_d allows the control of the input active power.

Working with unity power factor means to keep $i_q = 0$. The i_d current reference is provided many times by the output of a proportional-integral (PI) controller for the DC bus voltage control (Figure 11.17), as this component has the role of active power transfer to the DC bus.

The modules *Compensation, Voltage limit, and Transform* will be explained later in this chapter. The PWM module has to transform the reference voltage orthogonal co-ordinates into six gating signals for the power devices. A previous chapter for PWM algorithms showed several solutions for the DC/AC conversion. All of them can be redesigned for the grid interface application as they can be reduced to a set of reference voltages to be transformed into gate pulses. A group of methods are based on a conversion from the orthogonal system in phase reference voltages followed up by a comparison with a carrier waveform.

The space vector PWM concept allows better utilization of the DC bus voltage compared to carrier-based PWM methods and it represents, hence, a most convenient selection. The maximum voltage achievable at the power converter input is:

$$V_{1a}^{\max} = 0.61 V_{DC} \tag{11.21}$$

It is important to be able to have a large input voltage for the dynamic range of the system. The more the voltage available to be applied to the boost inductors, the

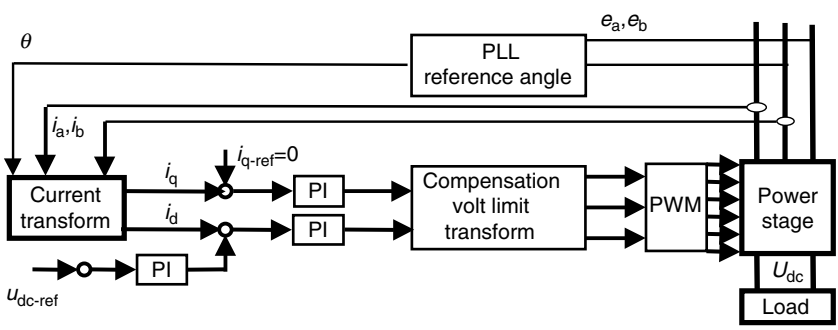


FIGURE 11.17 Base control structure.

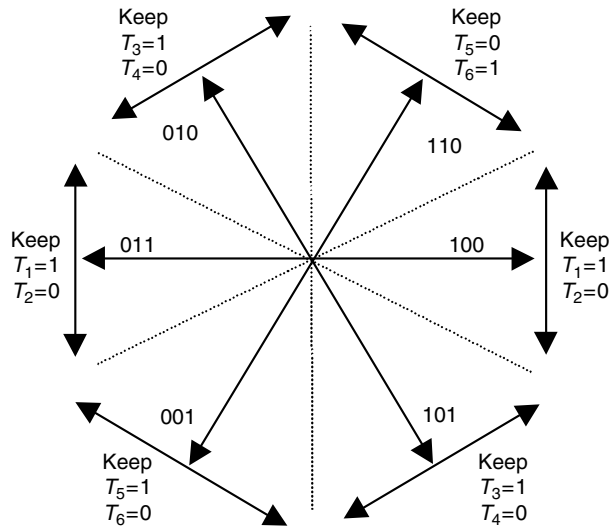


FIGURE 11.18 Switching vectors and definition of the no-switching intervals.

faster transients can be achieved. Full analysis of the closed-loop options is later included.

According to this SVM method, any set of instantaneous three-phase voltages can be obtained by switching the inverter between six active states defining the six-step operation and the null states in order to approximate a uniform rotation of the space vector corresponding to the three-phase input voltage system. Any desired position of the space vector in the complex plane is calculated by weighed addition of the neighboring switching vectors.

After the time intervals have been defined, there are several possibilities to distribute the active states over the sampling period. An interesting alternative does not switch each device for 60° on each fundamental cycle. This has also been discussed in Chapter 5 for generic PWM algorithms. As the input-phase current should be in phase with the input-phase voltage, the 60° no-switching interval should be chosen around the inverter-switching vectors (Figure 11.18). The main waveforms corresponding to this operation are presented in Figure 11.19.

11.3 CLOSED-LOOP CURRENT CONTROL METHODS

11.3.1 Introduction

As shown in Figure 11.17, the most important module of the control system consists of the closed-loop current controllers. The model of the system is expressed by Equation (11.19) and PI controllers are considered on each axis. As Equation (11.19) is different for each axis, different approaches to compensate the

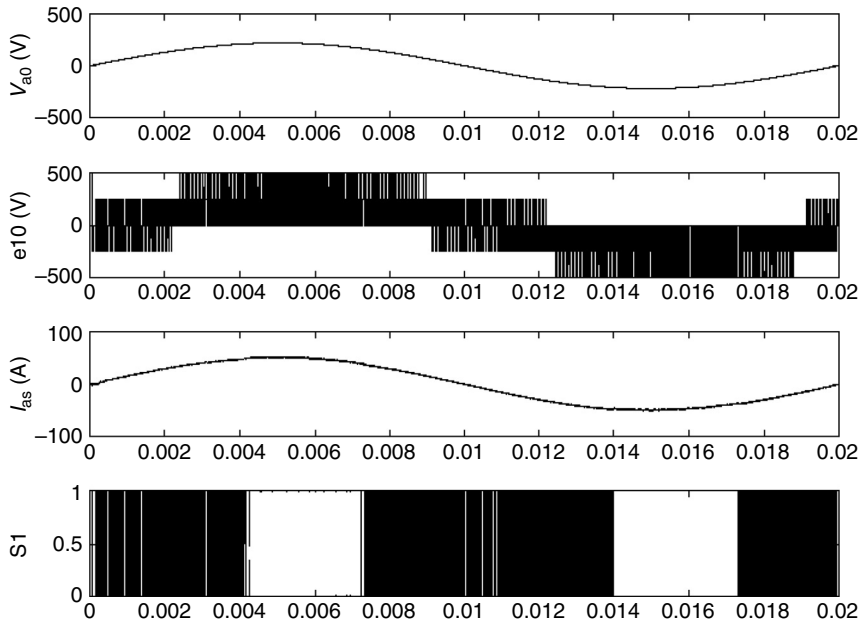


FIGURE 11.19 Waveforms characterizing the modulation with no-switching for 60° over a fundamental cycle.

cross-coupling terms are considered. Such terms are considered within the following module at the output of the PI current controller.

11.3.2 PI Current Loop

The PI current loop should be designed mainly to compensate the load voltage produced by the boost inductance term of Equation (11.19). A schematic representation is given in Figure 11.20.

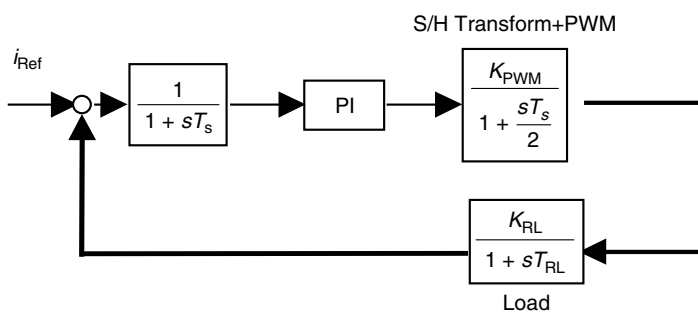


FIGURE 11.20 Schematics of the PI control system.

There are many methods to define the gains for the PI control and they are reviewed in Chapter 8. A simplified approximation is given here based on the boost circuitry parameters. The condition of unity gain of the closed-loop transfer function leads, after some calculation, to the values of the PI gains:

- Gain of the integrative term

$$k_{\mathrm{I}} = \frac{T_{\mathrm{RL}}}{2K_{\mathrm{RL}}T_{\Sigma}} = \frac{T_{\mathrm{RL}}}{2K_{\mathrm{RL}}\left(T_s + \dfrac{T_s}{2}\right)} \tag{11.22}$$

- Gain of the proportional term

$$k_{\mathrm{P}} = \frac{T_s}{2K_{\mathrm{RL}}T_{\Sigma}} = \frac{T_s}{2K_{\mathrm{RL}}\left(T_s + \dfrac{T_s}{2}\right)} \tag{11.23}$$

The concept of the vectorial control of three-phase power converters has already been discussed in Chapter 5. The application to grid interface systems encounters some limitations in the transient response performance due to limited voltage available across the boost inductance. A derivative of a direct application of the PI control without any special compensation is that the transient response time for input current step-up is shorter than the transient response time for the current step-down and the latter can be bothersome in many cases.

11.3.3 Transient Response Times

On the basis of PI gains, one can calculate the minimum response time for step-up or step-down transitions. As the resistive component is very small, the term R_{ri} can be even neglected. Owing to the largely inductive character of the load, a fast transient of the active current can be achieved with a large voltage applied across the boost inductance.

As the first equation in Equation (11.19) contains the E term, there are two different cases for analysis depending on the sign of the current change:

- Step-up: In order to increase the active current (i_d), it is necessary to provide the minimum available voltage across L_r (Figure 11.21). The response time will be small and it yields:

$$\Delta T_{\mathrm{up}} \approx L_r \frac{|\Delta i|}{E + |V_{\max}|} \tag{11.24}$$

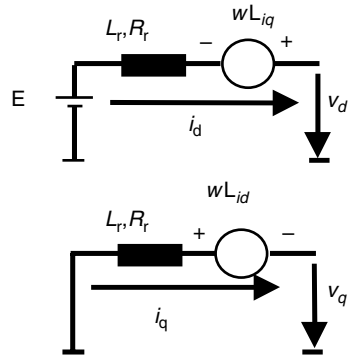


FIGURE 11.21 Equivalent circuits for d and q-axes.

- Step-down: In order to decrease the active current (i_d), it is necessary to provide the maximum available voltage across L_r. The response time yields:

$$\Delta T_{\text{down}} \approx L_r \frac{|\Delta i|}{|V_{\max}| - E} \tag{11.25}$$

11.3.4 Limitation of the (v_d,v_q) Voltages

It is easy to notice that different step-up and step-down time intervals are achieved with a smaller value for the step-up transient time. The step reference to the PI controller will have the tendency to force the output of the controller at a higher than possible value. Usually, a software limitation block is included as presented in Figure 11.22. This figure also illustrates the PI implementation in the context of Equations (11.19). The cross-coupling terms and the E term are also included. The cross-coupling terms are taken from the current feedback, but an alternative would be the reference currents.

It is important to note that many implementation solutions of the PI control of the grid interface converter use control systems similar to the motor control ones, without the term E. The problem with such an approach is that the dynamic range at the output of the PI controller is limited further by working with the voltage v_{d^*} component always close to the E value. The digital range for voltage may also be close to the value of E and the output of the PI controller may saturate digitally by reaching the end of its range. Figure 11.23 shows results for the control structure defined with Figure 11.22.

A multitude of solutions is reported in the technical literature to overcome this problem by artificially augmenting the voltage available to be applied across the input boost inductor [12,13]. Observing Figure 11.21 and Equations (11.19) defines two easy approaches to increase the maximum available voltage at the converter input:

- Using the cross-coupling terms
- Overlooking the PI outputs and applying all the maximum available voltage during transients

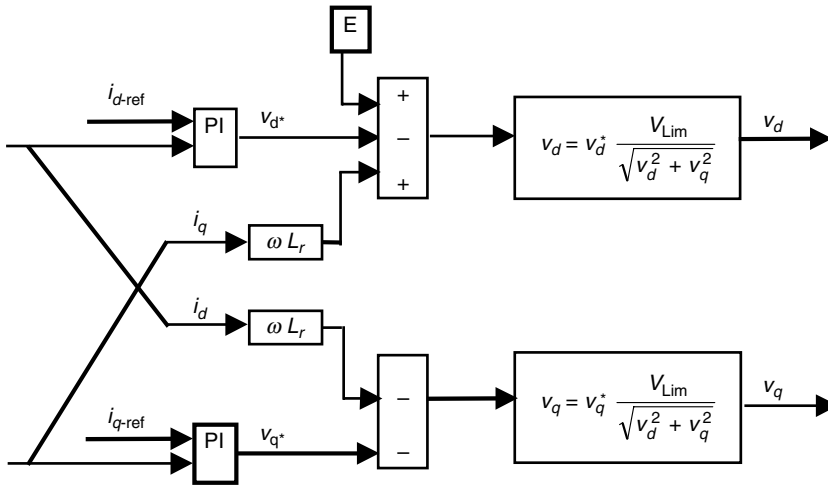


FIGURE 11.22 Schematic of the usual control with limitation.

11.3.5 Minimum Time Current Control

The *minimum time current controller* leads to excellent performance by finding the optimal control voltage to track the reference current with minimum time based on the optimal control theory. However, the applicability of this method is jeopardized by the large computational burden. The minimum time current controller is very similar to the following solution that will be discussed in more detail.

11.3.6 Cross-Coupling Terms

The cross-coupling term ($\omega L_r i_q$) [13] of Equations (11.19) is used to increase the voltage capability by increasing the i_q-axis current during a step in the active current i_d. In this case, the i_q current is used to maximize the applied voltage on the inductance L_r. Pushing a high i_q current while respecting $i_{q2} + i_{d2} \leq I_{d\max}$ can increase the term ($\omega L_r i_q$) and improve the voltage capability on the active current (i_d) axis. The unity power factor is given up during transients.

The increase in voltage can be expressed as:

$$\frac{\Delta v}{V_{\text{Lim}}} = \frac{\omega L_r i_q}{0.61 U_{\text{DC}}} \tag{11.26}$$

Results for step-up and step-down transients of the active current while applying the method shown in Figure 11.24 are shown in Figure 11.25.

Changing the i_q current reference or working with current on the q axis requires voltage to be applied on this axis (v_q). As the maximum available voltage is at any moment limited by the maximum radius of the space vector trajectory in the complex plane, a voltage applied on the q-axis may reduce the maximum voltage

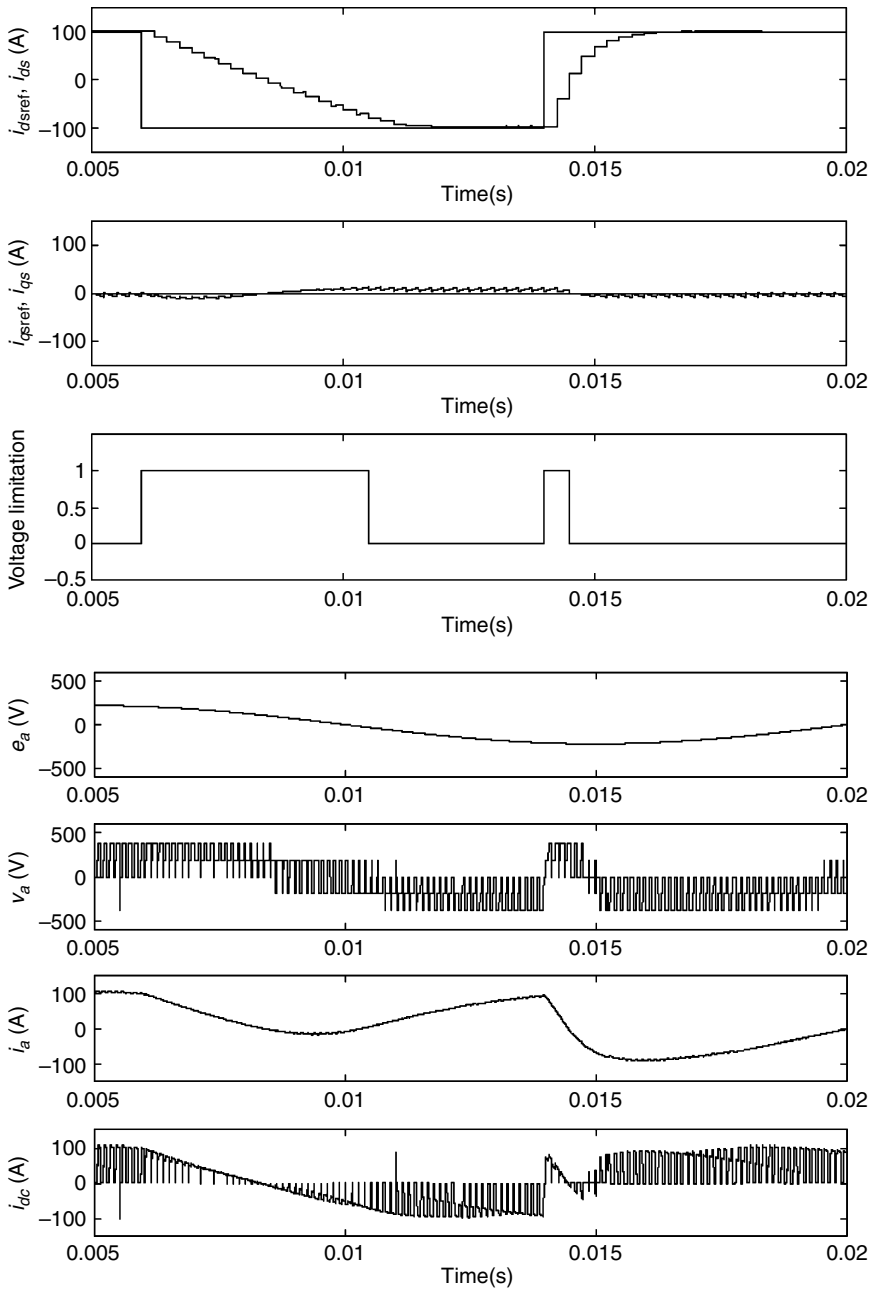


FIGURE 11.23 Simple current controller with voltage limitation for $L_r = 2.5$ mH, $R_r = 0.1\Omega$, $V_{dc} = 570$ V, $E = 220$ V, $f = 50$ Hz. (From Neacsu DO. IEEE International Symposium on Industrial Electronics, Bled, Slovenia, July 1996, 12–14, pp. 527–553, IEEE Paper 0-7803-5662-4/99. With permission.)

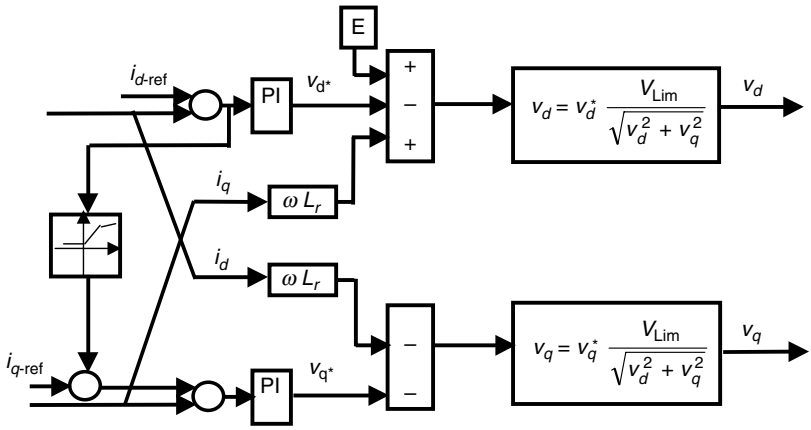


FIGURE 11.24 Schematic of the control system using cross-coupling terms.

available on the *d*-axis, and this jeopardizes somewhat the merits of this method. For this reason, an alternative is next analyzed by applying all voltage on the *d*-axis and suspending temporarily the effect of the PI control at large current errors.

11.3.7 Application of the Whole Available Voltage on the *d*-Axis

The limit of the maximum available voltage is generally expressed as

$$v_d^2 + v_q^2 = V_{\text{Lim}}^2 = (0.61 U_{\text{DC}})^2 \tag{11.27}$$

When applying all the voltage on the *d*-axis, $v_d = \text{V}_{\text{Lim}}$, $v_q = 0$ and the *q*-axis current is negative from Equations (11.19), this will further help to increase the *d*-axis voltage.

Rewriting Equations (11.19) for the case presented in Figure 11.26 and neglecting the voltage drop across the resistance in the boost circuitry yields:

$$\begin{aligned} E - V_{\text{Lim}} &= L_r \frac{\text{d}i_d}{\text{d}t} - \omega L_r i_q \\ 0 &= L_r \frac{\text{d}i_q}{\text{d}t} + \omega L_r i_d \end{aligned} \tag{11.28}$$

Solving this system yields the solutions:

$$\begin{aligned} i_d(t) &= I_d \cos \omega t - \frac{V_{\text{Lim}} - E}{\omega L_r} \sin \omega t \\ i_q(t) &= -I_d \sin \omega t + \frac{V_{\text{Lim}} - E}{\omega L_r} (1 - \cos \omega t) \end{aligned} \tag{11.29}$$

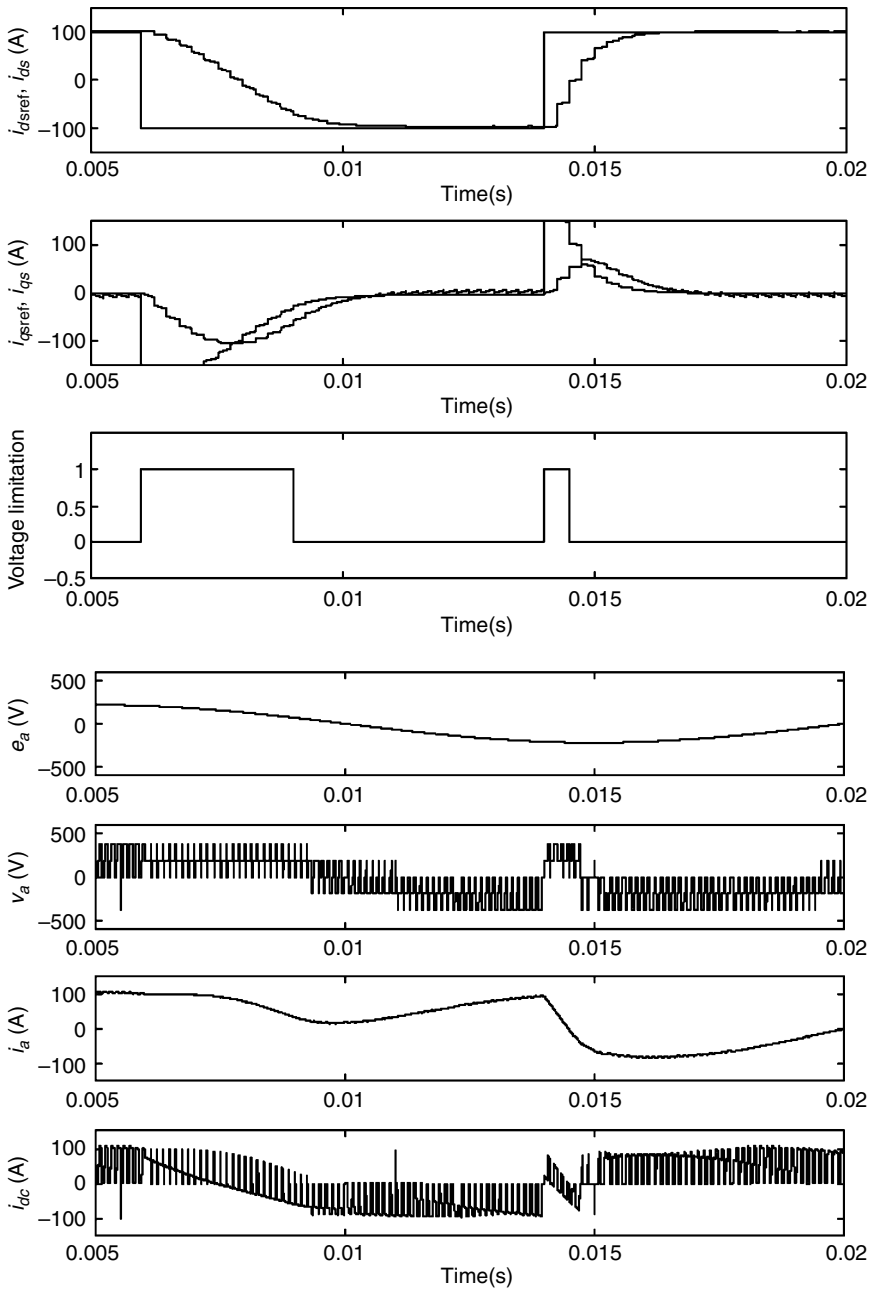


FIGURE 11.25 Current controller with $d-q$-axis cross-coupling for the case $L_r = 2.5$ mH, $R_r = 0.1\Omega$, $V_{DC} = 570$ V, $E = 220$ V, $f = 50$ Hz. (From Neacsu DO, IEEE International Symposium on Industrial Electronics, Bled, Slovenia, July 1996, 12–14, pp. 527–553, IEEE Paper 0-7803-5662-4/99. With permission.)

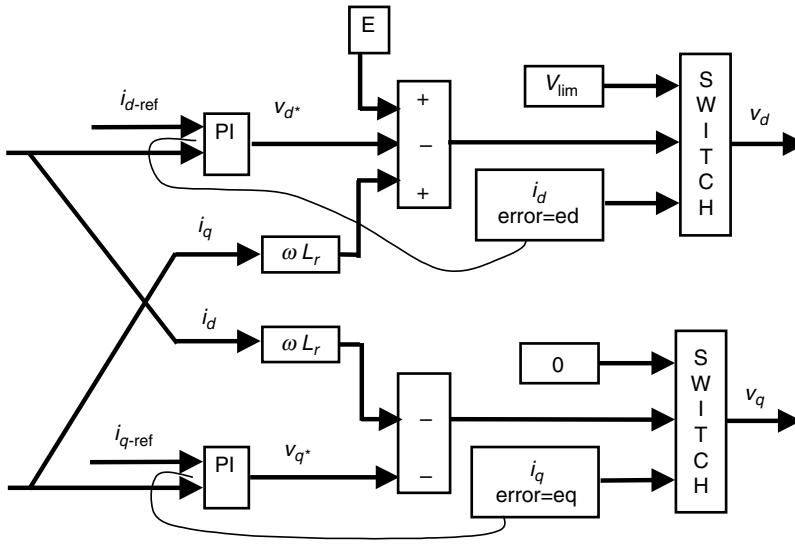


FIGURE 11.26 Control schematic for a system with application of the whole available voltage on d-axis during transients.

The response time for a step-down transient from I_d to $-I_d$ can be calculated by imposing the condition $i_d(\Delta T) = -I_d$. Figure 11.27 presents a theoretical response without taking into consideration the sampling effect.

It is very interesting to note that a step-down current modification from I_d to $-I_d$ brings i_q back to zero, and this will not jeopardize the behavior of the i_q current controller when this is again engaged [11].

Figure 11.28 shows results for the application of the entire voltage on d-axis during a transient. A comparison can be made between Figure 11.23 and Figure 11.25. At larger values of the i_d current, applying the whole available voltage on the active current axis leads to better results. As discussed before, the solution involving the cross-coupling terms requires some voltage on the q-axis to form the current i_q and the remaining voltage on the d-axis is reduced. Furthermore, asking for step modifications in both axes can produce instabilities during and following a transient.

11.3.8 Switch Table and Hysteresis Control

Fast current transients can be achieved with hysteresis control instead of PI control. Accounting for the symmetries within the three-phase systems, hysteresis control is considered for the two orthogonal (x, y) components of the grid current.

A novel hysteresis method in the synchronous reference (d, q) is introduced in Figure 11.29 and Table 11.2. The major advantage of this method, in comparison with the conventional stationary reference for the hysteresis control, consists in its

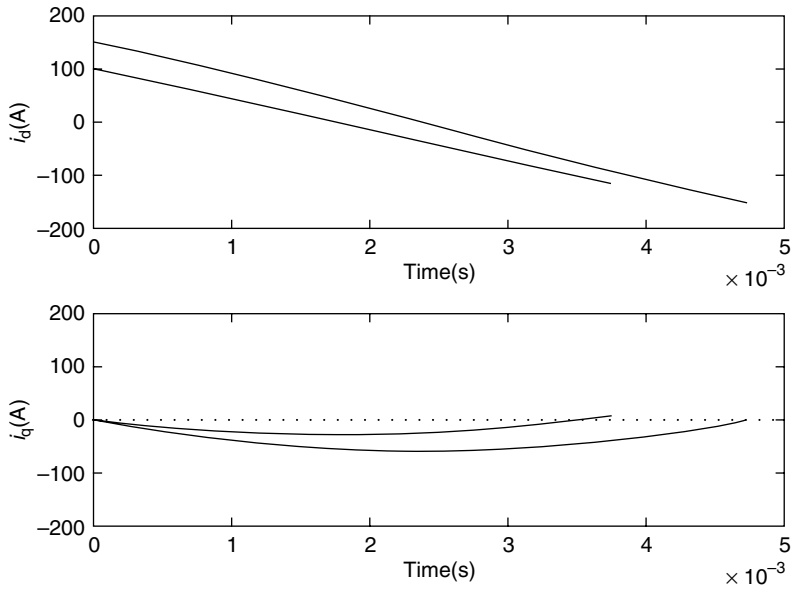


FIGURE 11.27 Theoretical response at i_d current step-down (100 A to −100 A and 150 A to −150 A) for $L_r = 2.5$ mH, $R_r = 0$, $V_{DC} = 570$ V, $V_{lim} = 0.61 * V_{DC}$, $E = 220$ V. (From Neacsu DO. IEEE International Symposium on Industrial Electronics, Bled, Slovenia, July 1999, 12–14, pp. 527–553, IEEE Paper 0-7803-5662-4/99. With permission.)

simplified implementation in vector-control systems. Current double-level hysteresis control in (d, q)-axes produces logic signals (y_d, y_q) that can uniquely be converted in (v_d, v_q) components of the voltage at the converter input. The sampling frequency can also be limited. The switch table is employed to select the switching vector closest to the coordinates (v_d, v_q) resulting from this algorithm (Figure 11.30 and Figure 11.31). As an alternative, this method can be applied with or without employing the cross-coupling terms. In a sense, this method is the equivalent of direct torque control used for the AC machine drives.

11.3.9 Phase Current Tracking Methods

Single- and three-phase grid connected power converters can also be controlled in a stationary reference frame directly employing phase or sinusoidal currents. The current control system reduces to a PI controller with a sinusoidal reference (Figure 11.32). Unfortunately, this type of system has been proven to introduce a nonzero steady-state error. To mitigate this issue, a solution based on an internal model principle [14] is discussed.

Let us consider a sinusoidal reference

$$i_R = I_R \cos(\omega t) \tag{11.30}$$

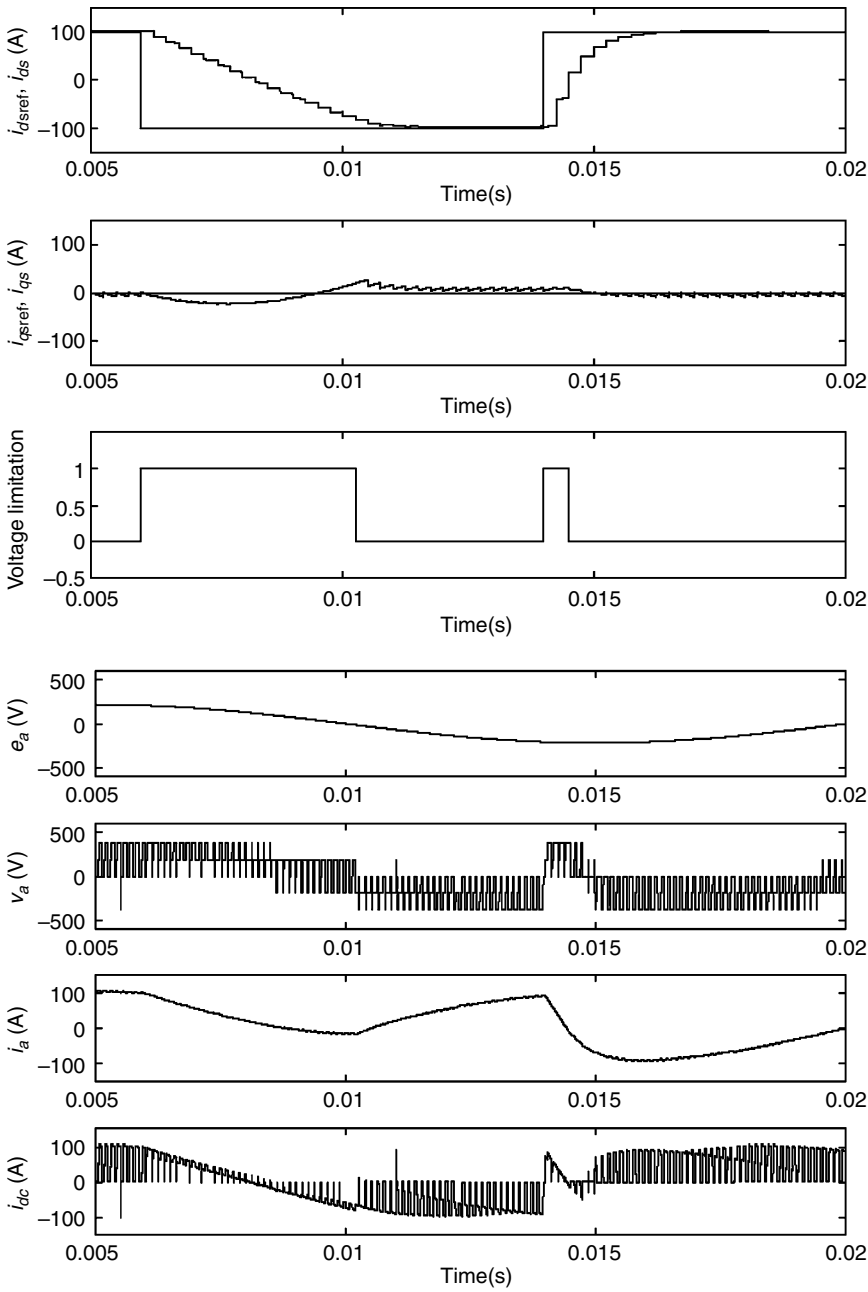


FIGURE 11.28 Whole voltage on d-axis for the case $L_r = 2.5$ mH, $R_r = 0.1\Omega$, $V_{DC} = 570$ V, $E = 220$ V, $f = 50$ Hz. (From Neacsu DO. IEEE International Symposium on Industrial Electronics, Bled, Slovenia, July 1996, 12–14, pp. 527–553, IEEE Paper 0-7803-5662-4/99. With permission.)

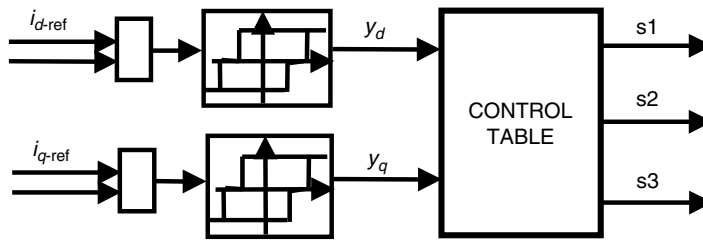


FIGURE 11.29 Schematics of the hysteresis control in a synchronous frame.

with the *Laplace* transform

$$I_R(s) = \frac{I_R s}{s^2 + \omega_0^2} \tag{11.31}$$

The *Laplace* transform for the error signal can be expressed as:

$$E(s) = \frac{I_R(s)}{1 + G_0(s)} = \frac{I_R s}{s^2 + \omega_0^2} \frac{1}{1 + G_0(s)} \tag{11.32}$$

where $G_0(s)$ represents the open-loop transfer function of the control system.

We would like to find the optimal form of the open-loop transfer function able to cancel the effect of the two imaginary poles ($\pm j\omega_0$) introduced by the sinusoidal reference term. In this respect, the open-loop transfer function is written as a ratio

TABLE 11.2
Switching Table (θ Represents the Angle of the Grid Voltages)

y_d	y_q	v_d	v_q	Choose Closest Vector to the Angle
−1	−1	+	+	$\theta + \pi/4$
−1	0	+	0	θ
−1	1	+	−	$\theta - \pi/4$
0	−1	0	+	$\theta + \pi/2$
0	0	0	0	Zero vector
0	1	0	−	$\theta - \pi/2$
1	−1	−	+	$\theta + 3\pi/4$
1	0	−	0	$\theta - \pi$

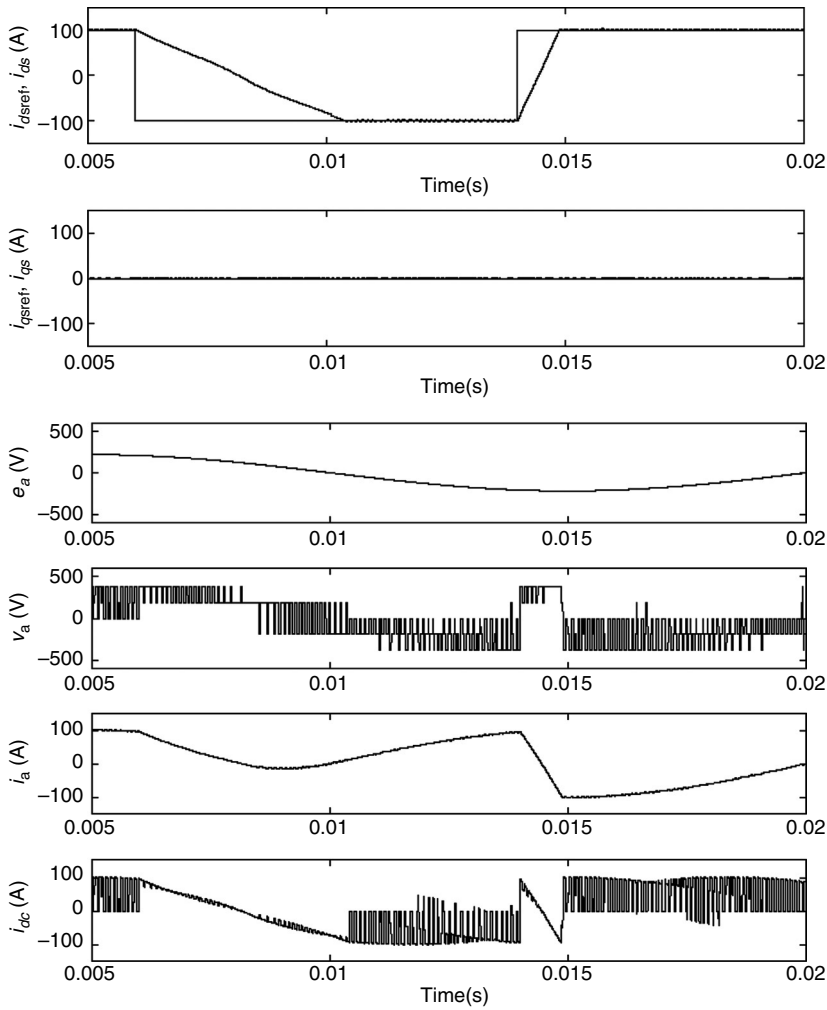


FIGURE 11.30 Switch table and hysteresis control for the case $L_r = 2.5$ mH, $R_r = 0.1\,\Omega$, $V_{DC} = 570$ V, $E = 220$ V, $f = 50$ Hz. (From Neacsu DO. IEEE International Symposium on Industrial Electronics, Bled, Slovenia, July 1996, 12–14, pp. 527–553, IEEE Paper 0-7803-5662-4/99. With permission.)

of polynomials with real number coefficients.

$$G_0(s) = \frac{N(s)}{D(s)} \Longrightarrow \frac{1}{1 + G_0(s)} = \frac{D(s)}{D(s) + N(s)} \tag{11.33}$$

$D(s) = 0$ should have the same solutions $(\pm j\omega_0)$ in order to cancel the effect of the sinusoidal reference. Moreover, $(\pm j\omega_0)$ should not be at the same time solutions of

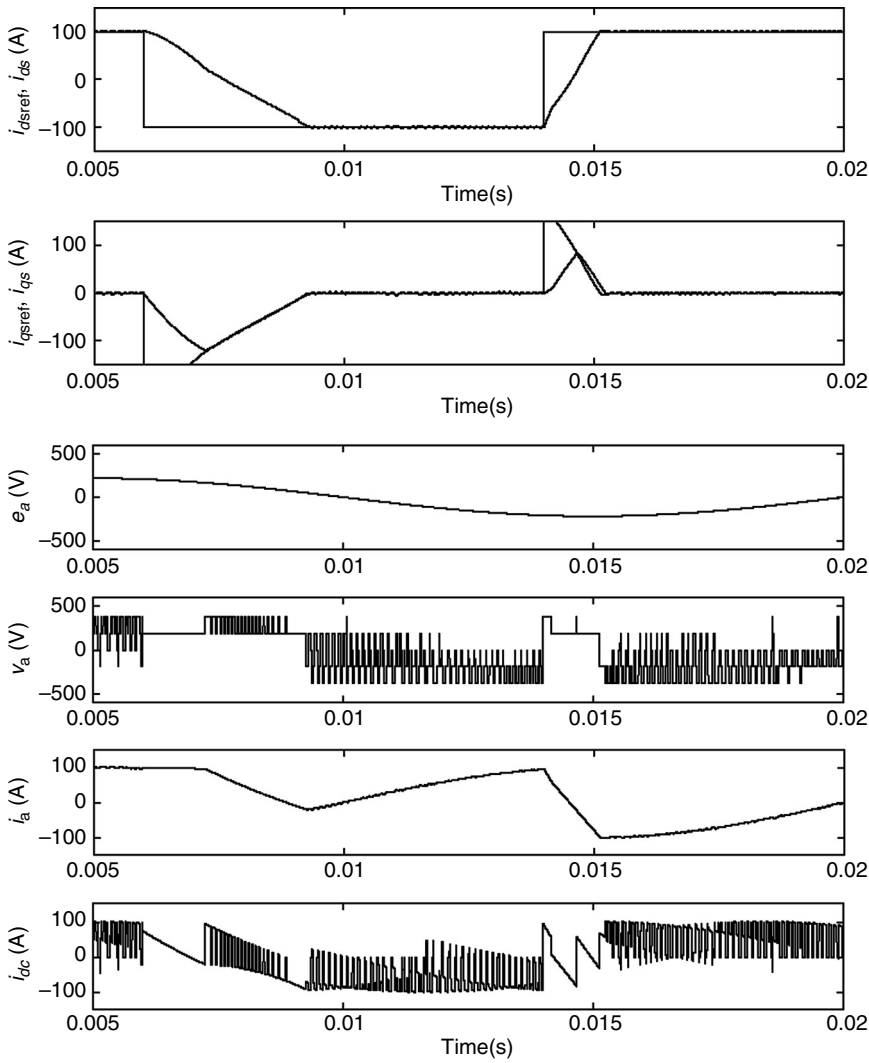


FIGURE 11.31 Switch table and hysteresis control using cross-coupling terms for the case $L_r = 2.5$ mH, $R_r = 0.1\,\Omega$, $V_{DC} = 570$ V, $E = 220$ V, $f = 50$ Hz. (From Neacsu DO. IEEE International Symposium on Industrial Electronics, Bled, Slovenia, July 1996, 12–14, pp. 527–553, IEEE Paper 0-7803-5662-4/99. With permission.)

$N(s) = 0$. This guarantees the elimination of the complex number solutions and the reduction of the steady-state error to zero.

The implementation of this control method is shown in Figure 11.33. The conventional PI regulator is enhanced by a term corresponding to the two imaginary solutions ($\pm j\omega_0$).

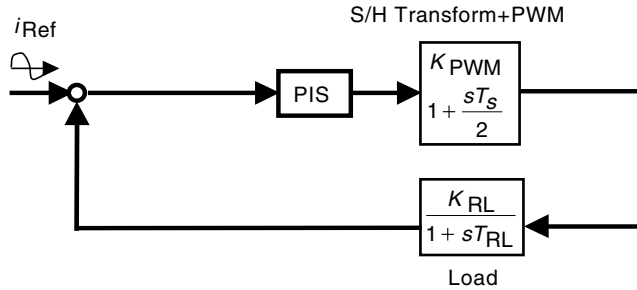


FIGURE 11.32 Schematics of the PI control system.

The equivalent transfer function of the regulator becomes:

$$G_{\mathrm{PIS}}(s) = K_{\mathrm{p}} + \frac{K_i}{s} + \frac{K_{\mathrm{s}} s}{s^2 + \omega_0^2} = \frac{K_{\mathrm{p}} s[s^2 + \omega_0^2] + K_i[s^2 + \omega_0^2] + K_{\mathrm{s}} s^2}{s[s^2 + \omega_0^2]} \tag{11.34}$$

The open-loop transfer function is calculated as:

$$G_0(s) = G_{\mathrm{PIS}}(s) G_{\mathrm{INV}}(s) G_{\mathrm{LOAD}}(s) \tag{11.35}$$

$$G_0(s) = \frac{F_1(s)}{[s^2 + \omega_0^2] F_2(s)} \tag{11.36}$$

and

$$E(s) = \frac{I_{\mathrm{R}} s}{s^2 + \omega_0^2} \frac{1}{1 + G_0(s)} = \frac{I_{\mathrm{R}} s}{[s^2 + \omega_0^2] F_2(s) + F_1(s)} \tag{11.37}$$

$E(s)$ has no imaginary poles introduced by the sinusoidal reference. It can be observed that $(\pm j\omega_0)$ are imaginary poles of $G_0(s)$ as proposed by the new control algorithm.

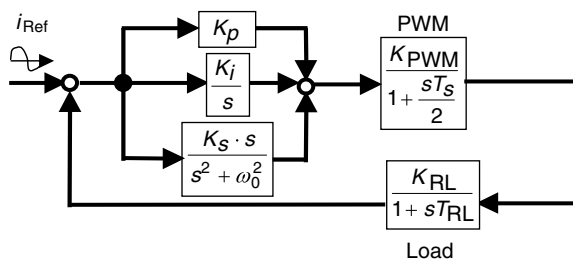


FIGURE 11.33 Block diagram of the compensated controller.

11.4 GRID SYNCHRONIZATION

Grid-connected power converters are seen as a current source by the grid while the input voltages are defined by the grid. This implies a synchronization of the PWM pattern with the phase of the grid in order to control the power factor. There are different methods based on a PLL circuit that are used to achieve grid synchronization.

The simplest solution used to synchronize the control of a single-phase grid-connected power converter consists in a zero-crossing detector followed by a counter circuit (Figure 11.34).

The grid voltage is sensed before any filter associated with the power converter and reduced to a lower level with a signal transformer or resistive divider. The resulting signal is compared against a threshold device, such as the base-emitter junction of a bipolar transistor or an IC comparator. This provides a logic signal corresponding to the alternating of the grid voltage. There are several sources of errors in this detection, including the noise in the line voltage due to unfiltered switching, dispersion and temperature variations of the threshold level, or delay in detecting the exact zero-crossing moment. However, these errors are generally smaller than the quantization step of the digital system.

The edges of the detected logic signal reset a digital counter that accounts for the phase coordinate of the PWM pattern. Improved systems include a phase-locked loop configuration able to filter unwanted small variations in the detecting process. This helps eliminating the jitter around the zero-crossing moments.

Let us consider a synchronization scheme based on a PLL circuit. A generic PLL circuit schematic is shown in Figure 11.35 and it is composed of a voltage-controlled oscillator (VCO) working at a frequency multiple of N times the detected frequency. In power converters, it makes sense to select the VCO frequency equal to the sampling frequency of the PWM pattern (Figure 11.36). The resulting train of pulses is divided by N resulting in a logic signal with a frequency comparable

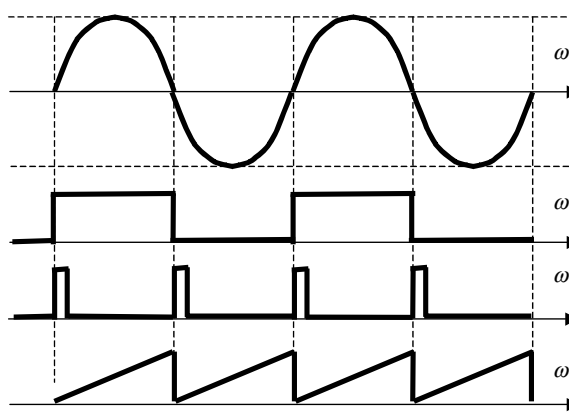


FIGURE 11.34 Principle of a simple synchronization circuit.

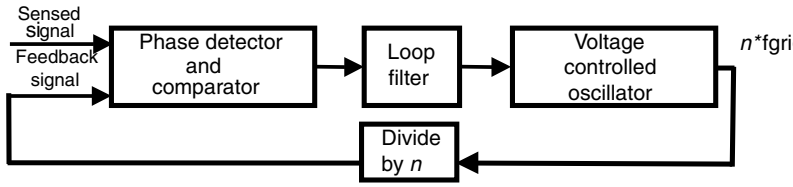


FIGURE 11.35 Principle of a PLL circuit.

with the sensed voltage. A phase detector compares the phase of the sensed and feedback voltages and it increases or decreases the control voltage accordingly. This control voltage is used as a reference for the VCO that modifies its frequency based on the phase difference. The goal of this closed-loop approach is to align the sensed signal with the generated one. If the frequency or phase of the sensed signal varies for any reason, this control loop acts as a filter and the feedback signal does not jitter. The feedback signal can further be used as a reference for the generation of the PWM pattern. Usually, the same counter is used both for closing the PLL loop and for counting the angular coordinate of the PWM pattern.

The major problem people face when implementing this PLL control in single-phase systems relates to the limited number of PWM cycles within one grid period. The discrete nature of the PWM-generation process limits the possibility of adjusting properly the controller phase. For instance, a converter with a 9 kHz switching frequency allows for 150 steps in the phase coordinate. The decision of the feedback

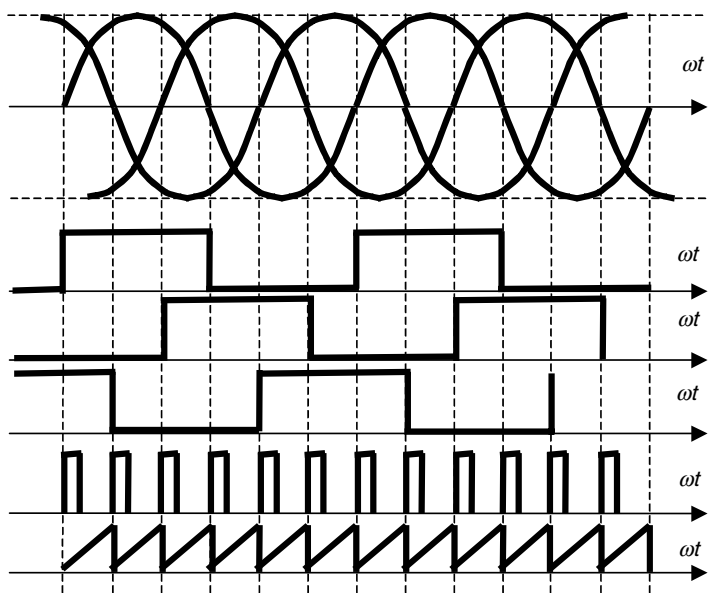


FIGURE 11.36 Principle of a simple synchronization circuit.

loop can only be to adjust the phase by ± 1 PWM pulse at a time. The effect is a possible step in the filtered voltage at each zero crossing when the phase is abruptly reset to zero. An alternative consists in using asynchronous PWM generators, but they do not guarantee the best harmonic content of the grid current. However, evolved systems can afford to work with asynchronous PWM that allows a noninteger ratio of switching and grid frequencies.

The PLL function can be implemented with dedicated analog or digital ICs or a proper software routine in the microcontroller or digital signal processor (DSP) control system. The frequency of the main signal is 50 or 60 Hz, which is very low compared to the performance of modern digital controllers. Therefore, a microcontroller implementation requires a zero crossing detector with direct interface to the digital hardware, a timer/counter counting with the clock frequency of the PWM sampling frequency, and a software routine running at the same sampling frequency.

Grid synchronization for three-phase converters benefit from multiple zero crossings and the symmetry of a grid generated three-phase system. The detection module includes zero-crossing detection for all three phases, and this results in a signal with a frequency six times larger than the grid frequency. The PLL circuit can therefore provide more resolution with a much finer tuning of the detected frequency.

Again the implementation can be achieved with analog or digital PLL ICs or with a software routine in the digital controller system.

11.6 PROBLEMS

P.11.1 Calculate the average and RMS values for the output voltage of rectifier systems shown in Table 11.1.

P.11.2 What is the effect of a line or grid inductance in the commutation process of the converter shown in Figure 11.2.

P.11.3 Draw the switching pattern of the GTO devices of Figure 11.3c to obtain the output voltage waveforms shown for both cases. How would you define the semiconductor loss for both control methods?

P.11.4 Consider the two topologies shown in Figure 11.7. What happens if the intermediate DC capacitor is missing? What should be the minimum value of this capacitor to maintain the operation as desired?

P.11.5 Compare the rating of the rectifier diodes in both solutions of Figure 11.8.

P.11.6 Compare the input filter-capacitor rating for the two solutions shown in Figure 11.10.

P.11.7 Following the example provided by Equation (11.3) through Equation (11.13), calculate the shapes of the current in the much simpler case of a single-phase converter and justify the second harmonic injection.

P.11.8 Compare the ratings of the IGBT devices used in building the power converters shown in Figure 11.10 and Figure 11.16, respectively, for the same grid-and-load conditions (say, 2 kW with a 120 V/60 Hz grid).

P.11.9 What are the drawbacks of neglecting the term E in the control system shown in Figure 11.22? Many people adapt their DSP control software from a

motor drive application to a grid-connected converter without adding up this term. The system apparently works, but at what risk? Can you complete this response with an imaginary example?

P.11.10 Determine the reasoning behind the switching sequence shown in Table 11.2 by using a vector diagram for both current and voltage.

P.11.11 Usually, practical systems of single-phase tracking control do not compensate for the sinusoidal reference. The system apparently works, but at what risk? Can you complete this response with an imaginary example?

P.11.12 Consider a single-phase grid-connected converter switched at 3.6 kHz, that is, a frequency ratio of 30. If the PWM generator maintains the synchronization between the generated PWM pattern and zero crossing, how big can be the steps in filtered voltage (or in the voltage reference for the PWM) at each zero crossing reset?

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