6 Practical Aspects in Building Three-Phase Power Converters

6.1 SELECTION OF THE POWER DEVICES IN A THREE-PHASE INVERTER

Previous chapters have explained the operation of a three-phase converter and the need for pulse width modulation (PWM). This chapter investigates the three-phase power converter as a system, outlining packaging and protection problems.

Power semiconductor devices for a three-phase power converter should be selected after determining the power converter ratings from the application requirements and taking into account the cooling and stress requirements for a given power level.

6.1.1 Motor Drives

When the power converter is used within a motor drive, its rating depends on the motor characteristics:

6.1.1.1 Load Characteristics

The application should provide information about the maximum torque required. The power converter should take into account an increase of about 60% torque availability as an overload. Sometimes, this overload is considered within the rated torque with a derate of the nominal torque.

6.1.1.2 Maximum Current Available

The maximum phase current can be derived from the nominal power on the motor data.

6.1.1.3 Maximum Apparent Power

The power converter must be able to process the whole apparent power, including the active power that produces torque and circulates reactive power.

6.1.1.4 Maximum Active (Load) Power

The maximum power processed by the power converter can be calculated if the efficiency and cos ϕ of the motor at a fixed operation mode are known. This criterion is not very effective as both these vary highly with the mode of operation.

After the motor data has been investigated for power converter ratings of maximum phase voltage and currents, selection of power semiconductor switches should be made including additional margins required for overvoltage and overcurrent.

6.1.2 Grid Applications

The power is transferred from the grid mainly on fundamental frequency and the power semiconductor switches can be rated for their active power and a tolerable power factor. The fixed grid voltage automatically sets a fixed maximum voltage on the power semiconductor switches. Both current and voltage can be considered, respectively, with overvoltage and overcurrent. Modern snubberless converters do not require an overvoltage rating consistently larger than the operation voltage across the power semiconductor device.

Once we have a rough idea of the maximum levels of currents and voltage on power semiconductor switches, we have to check the cooling system. Appropriate switching power or energy losses for the required current level can be calculated based on the device model or estimated from device datasheets. For instance, *Powerex* insulated gate bipolar transistors (IGBTs) provide all switching energy losses estimated for different operation conditions. The switching losses are added to the conduction losses of each power semiconductor device to determine the cooling requirements. The datasheet also provides information about the junction-to-case thermal resistance for each semiconductor package.

The application should also provide information about the cooling system (air or coolant) and the temperature and pressure of the coolant agent. Simple equations determine the change in temperature under these cooling conditions, when the power loss is known. If the system has to work at a high temperature, an iterative process in a larger power device should be considered. There are some cases when the thermal requirement becomes more important than the maximum current. For instance, a 27 kW/300 V/90 A IGBT based DC–DC power converter used in automotive applications may have the inlet coolant at 90°C. Selecting 100 A devices produces a junction temperature higher than recorded in the device datasheet. Iterative design leads to selection of 300 A devices in order to overcome this thermal constraint. Higher current devices have lower thermal resistance because they have a different technology and can cope better in high temperature conditions. In many cases, this solution is cheaper than considering a more sophisticated cooling system with a lower thermal resistance.

Power semiconductor devices should be protected against extreme operating conditions and faults. Several protection requirements have become standard for power converters at any power level.

6.2 PROTECTION

6.2.1 Overcurrent

A very large value of the current can pass through a power semiconductor switch for diverse operational reasons. Let us try to understand the main sources of overcurrent and the means of electronic protection before the fuses burn.

Insulation breakdown or wrong connections can produce a short-circuit between two output wires (phases) (Figure 6.1). A simple shunt resistor followed by a linear optocoupler or a Hall-effect sensor on the DC bus can detect the unexpected peak of the current. Another protection method consists of using the same phase current sensors that are used for current control. Each phase current is compared against two extreme thresholds for positive and negative levels.

Ground fault is another possible source of overcurrent, and it may be caused by a motor insulation breakdown to the ground (Figure 6.2). This source of overcurrent can also be detected with one of the previous methods: sensing either the DC current or each phase current. It is important to note that many industrial power converters controlled with vector-control methods do not measure all three-phase currents, but only two. They count on the symmetries of the three-phase system and calculate the third phase current as a difference between the sum of the other two currents and zero. Such a system cannot detect the ground fault if it occurs in the third phase. Accordingly, a ground fault-protected system must sense all the three-phase currents.

Another source of undesired large currents arises from the shoot-through or cross-conduction fault. In certain conditions, the turn-on of an IGBT can produce a large positive (dv/dt) across the other IGBT on the same leg. Due to the Miller effect, this voltage variation can be accidentally transformed into gate current and turn-on the second IGBT. This would produce simultaneous conduction of both IGBT devices and short-circuit of the DC bus (Figure 6.3).

A general approach for protection consists of sensing voltage across each IGBT to prevent voltage build-up when the IGBT is in a controlled ON state. There are

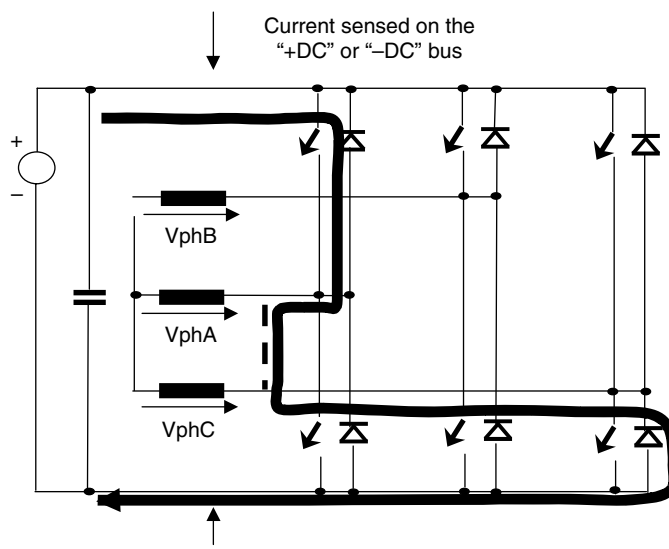

FIGURE 6.1 Short-circuit between two phases.

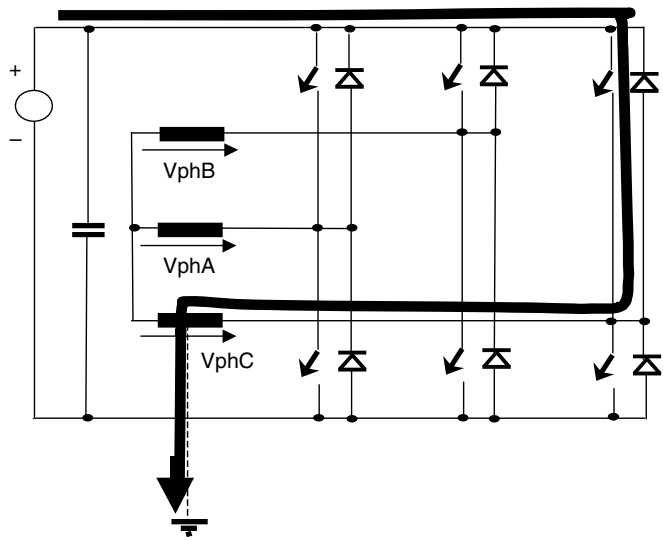

FIGURE 6.2 Ground fault.

many circuit possibilities to implement this method: all of them sense the collector–emitter voltage and compare it with a fixed reference. Exceeding the reference shuts the gates off.

A simple circuit designated for this protection is shown in Figure 6.4 and it is called *Desat protection*. This name comes from the bipolar transistor's saturation, and basically this circuit verifies if the controlled power semiconductor is really in the normal ON state (or "saturated" for a bipolar transistor). The voltage drop on the switch is sensed and compared with a reference defined by a Zener diode.

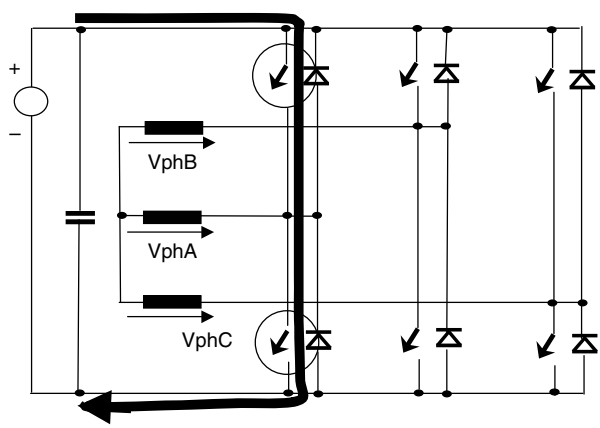

FIGURE 6.3 Shoot-through.

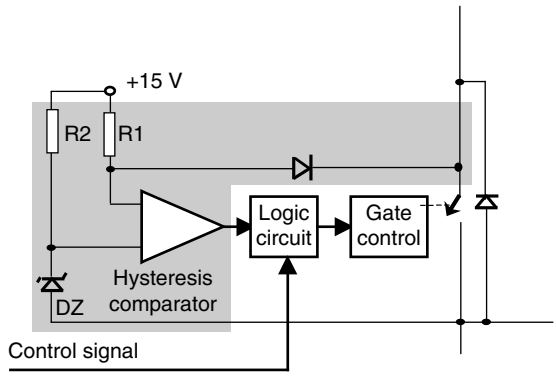

FIGURE 6.4 Desat protection.

If the transistor is unsaturated, the voltage drop is higher than the specified value, and the hysteresis comparator inhibits the control signal, turning-off the power semiconductor switch.

It is important to note that any of these three sources of overcurrent (line-to-line, ground, or shoot-through) can trigger the system protection in order to shut-off all six gates of a three-phase inverter. A quick shutdown generally produces a large voltage spike due to inductive components' tendency to keep the current circulating. This can be prevented by a *soft shutdown* of the IGBT under overcurrent, paying the price, though, of increased complexity of the control circuit.

The soft shutdown method shuts the gates off with a large gate resistor that is able to slow-down the turn-off waveforms. Synchronization of shutdown for all six gates implies additional complexity of the control circuitry. For this reason, the soft shutdown is used at low power levels where integrated circuits (IC) technology can easily accommodate the extra circuitry. International Rectifier Corporation has a nice series of high-voltage (600 and 1200 V) gate drivers (IR21xx and IR22xx) able to perform soft shutdown in the horsepower range.

6.2.2 Fuses

Processing power in high-voltage circuits implies also protection against overcurrent and, especially, short-circuits. Fuses represent the most known method of overcurrent protection. A fuse is a device able to break a high current through its own damage under the heat generated by that current. Figure 6.5 presents the structure of a fuse.

Current through the fuse produces heat, especially in the reduced sections. At high currents, these regions melt and the fuse is damaged. The rated current of the fuse is the maximum current carried continuously by the fuse without damage. This continuous current rating is defined with test procedures given in IEC269 or UL248 standards for ambient temperature, open air, and AC voltage at 50 or 60 Hz (grid).

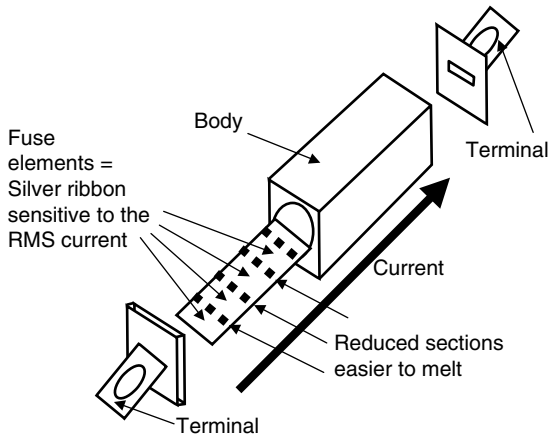

FIGURE 6.5 Basic structure of a fuse.

Another standard UL198L (DC Fuses for Industrial Use) provides the DC rating of the fuses in industrial applications.

An important parameter of a fuse is I^2t (squared RMS current multiplied by the clearing time) and it defines the fuse melting under a high fault current (Figure 6.6) [1]. The fuse can also melt when a lower current passes through the fuse for a longer time. This defines a dependency of the melting time that is inversely proportional to the applied current (Figure 6.7).

Selection of fuses for protection of a power converter depends on the voltage, total RMS current, the semiconductor device's rupturing I^2t value, device current di/dt, circuit inductance, ambient temperature, style of connection, and so on [1–3]. Diodes and other rectifier semiconductors are provided with datasheet information on a half-cycle surge rating characterized by the magnitude of a single sinusoidal half-cycle pulse at 50 or 60 Hz that the device can withstand. This value along with the half-cycle length (8.33 or 10 msec) is considered to calculate the semiconductor I^2t value.

Fuse selection is dependent on the total current containing both fundamental and harmonics and this is especially important in IGBT fusing. The high-switching frequency influences through the skin and proximity effects that are caused by

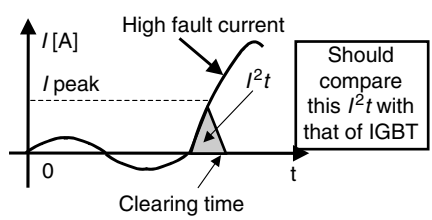

FIGURE 6.6 Fuse action on high fault current.

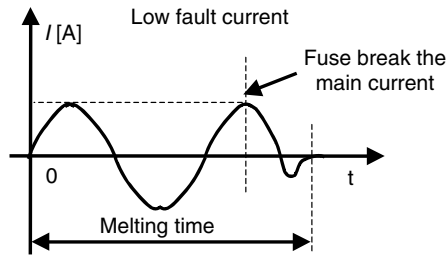

FIGURE 6.7 Melting of the fuse due to long-term current.

nonuniform distribution of current density in the fuse elements. These effects are not very clearly known or defined, but they may justify premature opening of the fuse under the switching frequency components. A complete analysis of the power dissipation in a fuse under harmonics is presented in [4].

When a short circuit occurs in an IGBT-based circuit, the collector–emitter voltage tends to increase immediately to a high value, which rapidly increases the internal power dissipation and failure of the device. Electronic protection circuits have been presented in the previous section. A fuse is used as protection when the electronic protection fails or is not used. The presence of the unprotected short-circuit in an IGBT can produce IGBT rupture, melting of the emitter connections or of the other circuit wires. If the IGBT rupture I^2t data is missing, a good practice is to calculate the I^2t for the copper bonding wire:

$$I^2t = (100{,}000, \ldots, 110{,}000)S^2 \tag{6.1}$$

where S is the wire section in square millimeter.

This will ensure lower values than those experimentally defined for the IGBT case.

There are several possible distribution of fuses within a power converter. A complete solution includes protection on the DC bus, on phase currents, and all IGBTs. This is not totally justified and a simpler or cheaper solution is generally satisfactory. The best compromise for the position of fuses within a three-phase inverter is shown in Figure 6.8.

When the fuse needs to break an inductive current within a DC circuit, the value of the circuit inductance determines the clearing time. The larger the inductance, the harder for the fuse to break the current. If a fuse is capable of suppressing a given amount of energy, then the DC voltage rating of a fuse is only valid for a specific time constant influenced by the amount of inductive component. For instance, a typical time constant for a capacitor bank, battery supply, and distribution circuits or UPS inverters is less than 10 msec; the DC motor armature has a typical time constant of 20–40 msec, and a traction system has a time constant of less than 100 msec.

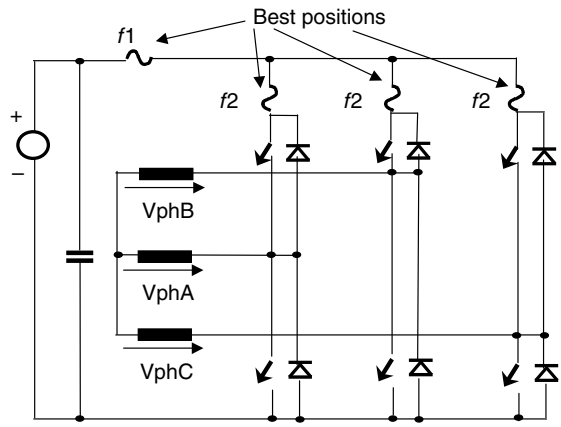

FIGURE 6.8 Best (reduced) placement of fuses.

6.2.3 Overtemperature

Power semiconductor devices are usually rated at a junction temperature between −40 and 150°C. Automotive, aerospace, or military applications require semiconductors rated below −40 or above 150°. For instance, power electronics for hybrid vehicles use the same cooling path as the engine providing a coolant at 90°. MOSFET devices are available today at 175 or 200° junction temperature. The advent of silicon carbide-based power devices will make possible operation above 250°.

A direct junction temperature measurement is very difficult. There are IGBT devices available in the market with junction temperature measurement based on a sensing diode on the same package, but they are expensive and, therefore, not widely used.

The most common approach to overtemperature protection consists of a temperature sensor on the cold plate or heatsink supporting the IGBT. If this thermocoupler is mounted as close as possible to the IGBT, it provides a good reading of the device package's temperature. The measurement circuit is followed by analog processing. Unfortunately, the thermocoupler sensor is not linear and a linearization curve is needed if the temperature really needs measuring. This can usually be achieved by software using a piece-wise linearization method. Overtemperature protection does not really need this linearization or precise measurement, but requires only a comparison with a reference threshold in order to trigger the shutdown process.

Additional temperature monitoring is needed for the cooling system: this is either air-based or liquid-cooled. Some systems cooled with liquid also check the pressure.

6.2.4 Overvoltage

DC bus voltage and phase voltages are also monitored. If overvoltage on the DC bus is detected, the IGBTs within the three-phase inverter need to be shutdown. Power

electronics systems may require monitoring of the phase voltages and shutdown in case of overvoltage. Circuits for voltage monitoring are based on resistive or transformer sensing of voltage followed by comparison with required thresholds. In high voltage, insulation with transformers from the power wires is required.

Except for these accidental overvoltage faults demanding fast action from the gate controller, overvoltage with slower transients are suppressed with devices called surge arrestors. This type of overvoltage can occur, for instance, at connection of a power electronics circuit to the power lines.

There are two classes of surge arresters: crowbar protection and clamping protection.

A crowbar device starts to conduct due to a quick change of its impedance when subjected to a large voltage. During this conduction interval, the voltage drop across the crowbar is limited to less than 15 V, allowing a large current to pass through it. It may be used in association with a dissipation resistor, a current-limiting device, or in series with a fuse that may blow due to the large current produced when the crowbar conducts. The energy is not dissipated on the crowbar device itself. The crowbar technique is also used in low-voltage DC/DC voltage regulators.

The most commonly used crowbar devices are air-gap protector, carbon-block protector, gas-discharge tube, and silicon-controlled rectifier (thyristor).

The second group of surge arrestors is composed of clamping devices. A clamping device varies its internal resistance to limit the voltage transient by absorbing some of the transient energy. This is a serious limitation during application at large currents. Possible devices in this group are Zener diodes and metal oxide varistors (MOVs).

MOV devices are mostly used in power converter applications. They have a voltage variable resistance and can support large currents during protection. However, they tend to degrade over time if high peak currents are repeated.

6.2.5 Snubber Circuits

The transition of current between a power semiconductor switch and a diode has been explained in Chapter 2. Once current has been transferred from the turning-off device to the turning-on device, the voltage starts to swing. This *hard-switching* induces a time interval during which both current and voltage are large in the turning-on device. As shown in Figure 2.2 and Figure 2.7, this stress is more important for inductive loads due to the overvoltage produced by the current variation (di/dt).

6.2.5.1 Theory

Trajectories in the (I_C, V_{CE}) corresponding to the real operation are shown in Figure 6.9. They depend upon stray inductances, parasitic capacitances, and IGBT switching performances as di/dt, dv/dt. For instance, the IGBT package itself has a stray inductance of few tens of nanohenries (nH) (for devices of the order of hundreds of amperes). The largest parasitic inductance is introduced by the DC bus connection of the inverter. It is very important to minimize the circuit parasitic inductances with a proper layout design.

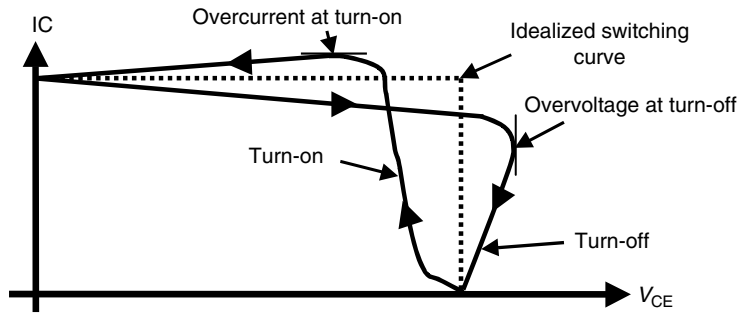

FIGURE 6.9 Trajectories during operation within a real circuit.

Factors as di/dt, dv/dt can be partly adjusted through the gate circuit and the operation area can be minimized inside the datasheet safe operating area. The overvoltage produced by the recovering diode can also be limited by increasing the gate resistor.

It may be necessary to limit the slope of the current at turn-on of a power semiconductor device by inserting a series inductance. This is not usually the case in modern devices, but is required for some gate turn-off thyristors (GTO) or bipolar transistor-based inverters. Since the switching current adds up to the recovery current of the diode, sometimes an alternative solution consists of using a saturable inductor with a ferrite core in series with the diode. This inductor is supposed to take over all the voltage during recovery and it may reduce the recovery current.

At turn-off, it may be necessary to limit the slope of the voltage. A better limitation along with power loss reduction can be achieved with *snubber* circuits (Figure 6.10). When the *snubber* circuit is missing, the voltage will resonate due to the semiconductor parasitic capacitance and connections' inductance. The *snubber* circuit has to dump these oscillations.

For low-power applications, the parasitic inductance of the IGBT package and mounting on the bus bar are smaller than the inductance of the DC link. This is the

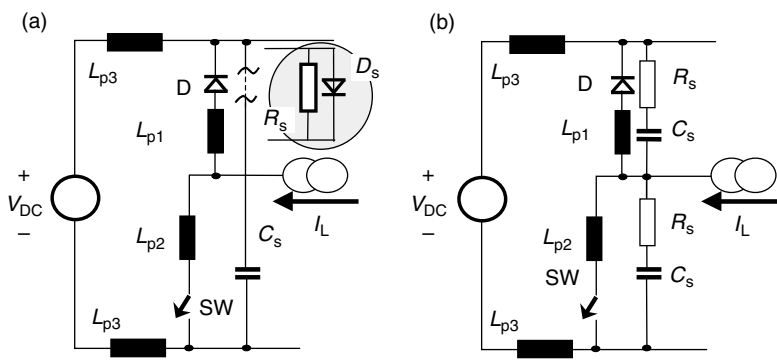

FIGURE 6.10 Snubber and switch equivalent circuit.

case of discrete IGBTs or IGBT-based power modules used in applications above tens of amperes. Using power modules is definitely better as all connections are inside the package with extremely low parasitic inductances. The common solution consists of a simple decoupling capacitor across the entire inverter leg, providing a noninductive path for current transition (Figure 6.10a). High-frequency polypropylene film capacitors or other low equivalent series inductance-capacitors are especially designed for dual module IGBTs. They are mounted directly on the module terminals (Table 6.1) [5].

Depending on the estimated equivalent parasitic inductance, the decoupling capacitor can have values between 100 nF and 10 μF, usually 1 μF for each 100 A in the power semiconductor switch. A simplified calculation of the capacitor value can be made after neglecting the turn-off details within the semiconductor (Figure 6.11). The collector–emitter voltage is given by:

$$V_{CE}(t) = V_{DC} - L_p \frac{di(t)}{dt} \Longrightarrow \frac{di(t)}{dt} = \frac{1}{L_p}[V_{DC} - V_{CE}(t)] \tag{6.2}$$

$$V_{CE}(t) = V_{DC} + \frac{1}{C_s}\int i(t)dt \tag{6.3}$$

It yields:

$$\frac{di(t)}{dt} = -\frac{1}{C_s L_p}\int i(t)dt \quad \text{with the solution } i(t) = I_o \cos\left[\frac{1}{\sqrt{C_s L_p}}t\right] \tag{6.4}$$

TABLE 6.1
Solutions for Special Snubber Capacitors

Code	Dielectric	Electrode	Voltage [V]	Capacitance [μF]	Max (dv/dt) [V/μsec]
		Package type: Wrap and Fill Axial leads			
WPP	Polypropylene	Foil	250–1000	0.001–2.0	300–10,000
DPF	Polypropylene	Foil	250–2000	0.001–0.47	3000–10,000
940-1	Polypropylene	Double metalized	600–3000	0.1–4.7	100–2,000
942-3	Polypropylene	Double metalized	600–2000	0.1–4.7	500–5,000
		Package Type: Dipped with Radial Leads			
CDx	Mica	Foil	500–1500	0.1–10 nF	>10,000
		Package type: direct mount on IGBT module terminals			
SCD	Polypropylene	Double metalized	600–2000	0.1–10.0	100–2,000

Source: Data compiled from the 2004 Cornier-Dubilier databook.

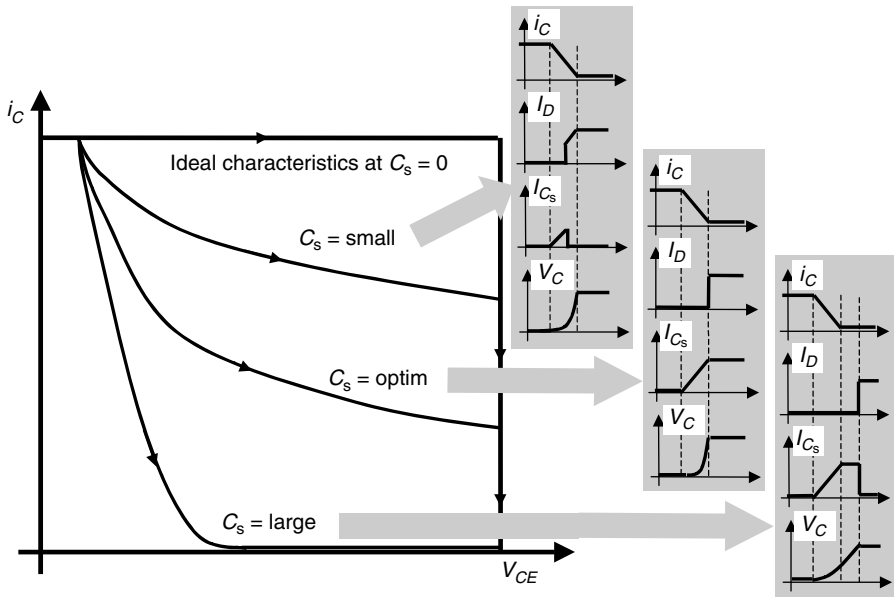

FIGURE 6.11 Calculation of the snubber capacitor value.

where I_o is the load current at the moment of turn-off. Replacing this solution in Equation (6.3) yields:

$$V_{CE}(t) = V_{DC} + I_o\sqrt{\frac{L_p}{C_s}}\sin\frac{t}{\sqrt{C_s L_p}} \tag{6.5}$$

One can define a maximum desired voltage across the IGBT [V_{MAX}] and replace the maximum defined by the previous equation.

$$V_{MAX} = V_{DC} + I_o\sqrt{\frac{L_p}{C_s}} \Longrightarrow C_s = L_p\left[\frac{I_o}{V_{MAX} - V_{DC}}\right]^2 \tag{6.6}$$

Therefore, calculation of the required capacitor value depends on the estimated value for the parasitic inductance.

Using the decoupling capacitor alone may not be the solution when the resonance between the DC link inductance and this capacitor produces a large bus ringing. An alternative solution is to insert a resistor-diode circuit in series with the capacitor. This will clamp the ringing. When the switch turns off, the energy stored within L_{p3} is transferred to the capacitor C_s. The tendency of returning the energy to the bus inductance through oscillation is blocked by diode D_s. Moreover, the capacitor is decoupled during turn-on and the DC link parasitic inductance will smoothen the turn-on transition and reduce the appropriate switching loss.

The drawback of this approach is the additional inductance introduced in the circuit by the resistor–diode connection.

For high-power applications, the solution presented in Figure 6.10b is used. The *snubber* contains an R_s–C_s series network across each power semiconductor switch. The C_s capacitance must be twice as large as the parasitic capacitance of the power semiconductor switch and its mounting. The R_s resistor is introduced to sustain the whole load current when C_s is discharged. Accordingly, it yields $R_s = V_{DC}/I_L$.

A second condition for R_s can be derived from the time constant for the discharging process. The snubber capacitor should discharge back to V_{DC} before the next turn-off moment, that is:

$$R_s = \frac{1}{6C_s f_{sw}} \tag{6.7}$$

The introduction of this resistor reduces system efficiency due to inherent losses. The resistor loss at turn-off yields:

$$P_{R_s}(\text{off}) = \frac{1}{2} C_s \left[V_{pk}^2 - V_{DC}^2 \right] f_{sw} \tag{6.8}$$

Losses at turn-on can be approximated as having the same value.

Using a resistor–diode assembly for dumping the voltage ring is another option. Advantages in this case are similar to those for clamping of the whole DC bus. The snubber capacitor is fully discharged during IGBT turn-on, whereas it is fully charged at turn-off. The losses in the snubber resistor are substantially higher in this case and can be expressed as:

$$P_{R_s}(\text{off}) = \frac{1}{2} C_s V_{pk}^2 f_{sw} \tag{6.9}$$

6.2.5.2 Component Selection

Snubber capacitors are subject to high peak and RMS currents as well as large dv/dt. The industry now provides capacitors especially built for this application. Snubber capacitors can be purchased as discrete components or as modules that allow connection of the snubber directly across the IGBT module terminal in order to minimize the terminal inductance. Table 6.1 presents different solutions for snubber capacitors provided by Cornell-Dubilier [5].

The snubber resistor should be selected to have the lowest possible inductance. Possible choices are carbon composite or metal film, but these are not easily available at high power. In this case, low inductance wire-wound resistors can be selected.

The diode in the snubber circuit experiences the same peak voltage as the snubber capacitor: the current is small in average but large in its peak. The blocking action of these diodes should be faster than the actual protected power semiconductor. Fast-switching diodes rated for the snubber capacitor voltage and circuit peak current should therefore be selected.

6.2.5.3 Undeland Snubber Circuit

Using Resistance-Capacitance-Diode (RCD) snubbers for both power semiconductor switches on one inverter leg requires many components and introduces large losses, as demonstrated. A special snubber circuit has been proposed by Undeland (Figure 6.12) to minimize the number of components and to reduce the losses within the snubber [23]. This circuit confines all losses in only one resistor, simplifying the energy recovery.

Capacitor C_{s2} separates the snubber circuit from the power stage during the intervals between switchings. At the end of each switching cycle, the excess energy within the inductance is discharged through D_{s2} and D_{s1} into the capacitor C_{s1}. The voltage across this capacitor tends to go above the DC bus voltage and the difference is dissipated on the snubber resistor R_s. This energy through R_s can be further recovered into the DC bus with regenerative snubbers.

6.2.5.4 Regenerative Snubber Circuits for Very Large Power

The higher the power within the power stage, the higher the losses in the snubber resistors associated with the six switches. For this reason, high-power converters are built with circuits that can recover something from this energy into the DC bus [6,7]. They are generally referred to as *regenerative snubbers* (Figure 6.13) [8–10].

It is worth noting that regenerative snubbers are useful in high-power converters equipped with slow-switching devices like gate turn-off thyristors (GTO) where losses are large. Such equipment is still in use in many places and some companies are currently producing GTO-based converters in multi-MW range. On the other hand, modern power semiconductor devices, for instance, IGBTs, are nowadays available in 1 kA range, and some of these devices do not need snubbering at all. Building snubberless power converters with IGBTs like Powerex MegaPack (300 V, 1000 A) makes this topic obsolete. However, due to historical reasons and due to the large number of GTO-based converters in use, regenerative snubbers are presented here.

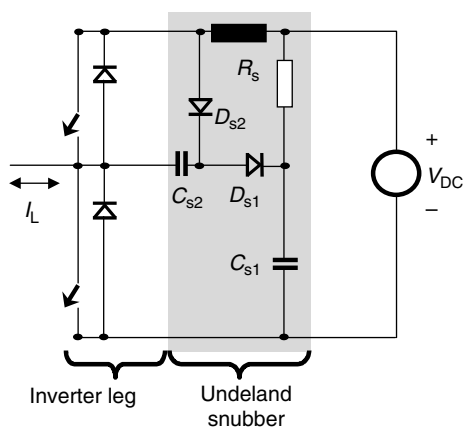

FIGURE 6.12 Undeland snubber with reduced losses.

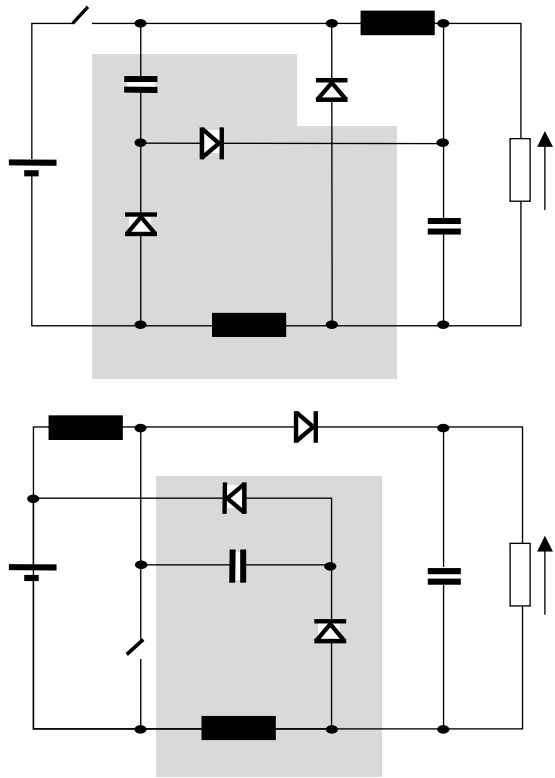

FIGURE 6.13 Circuit examples of regenerative snubbers.

6.2.5.5 Resonant Snubbers

The whole idea of using a snubber circuit can be reduced to controlling the slope of the current increase at turn-on and the slope of voltage at turn-off. The most minimal solution has been shown to be a series inductor for turn-on and a parallel capacitor for turn-off. Complete solutions including resistance and diodes have been explained. Another concept is that of keeping all the transition losses out of the power semiconductor device by controlling its switching at zero current or zero voltage. This concept was first developed in the 1980s and called *resonant snubber*. The simplest implementation of this concept consists of a circuit with a capacitor parallel to the power semiconductor device and an increased inductance in series (Figure 6.14).

This is represented as a buck converter, but it can also be a part of a converter leg. The capacitor might be the parasitic capacitor across a MOSFET device. The power semiconductor switch Sw1 will have transitions at zero voltage due to the resonance. It is controlled like regular switches within the buck or inverter leg operation.

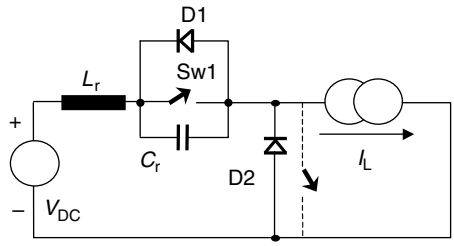

FIGURE 6.14 Principle of resonant snubbers.

Supposing Sw1 is OFF, the load current I_L passes through C_r and L_r charging the capacitor. Assuming a constant current I_L, the voltage across the resonant inductor stays zero whereas the capacitor voltage increases linearly:

$$V_{C_r} = \frac{I_L}{C_r} t$$

By difference, the voltage across D2 decreases as:

$$V_{D2} = V_{DC} - \frac{I_L}{C_r} t \tag{6.10}$$

Shortly, this diode turns-on and the charging time interval is defined as:

$$t_1 = \frac{V_{DC}}{I_L} C_r \tag{6.11}$$

It is important to note that the slope of the voltage increase across the switch Sw1 is ideally limited by resonance at I_L/C_r. The existence of the time interval t1 does not considerably change the operation of the converter.

Next, the diode D2 conducts a part of the load current while the rest of the current circulates through the series resonant circuit L_r–C_r. The voltage across the capacitor C_r is the solution of the differential equation:

$$L_r C_r \frac{d^2 v_{C_r}(t)}{dt^2} + V_{C_r}(t) = V_{DC} \tag{6.12}$$

with $V_{Cr} = V_{DC}$ as the initial condition.

The expression of the capacitor voltage yields:

$$V_{C_r}(t) = V_{DC} + \sqrt{\frac{L_r}{C_r}} I_L \sin\left[\frac{1}{\sqrt{L_r C_r}}(t - t_1)\right] \tag{6.13}$$

This shows an increase of the capacitor voltage after turning on the diode D2 and then a decrease towards zero according to the resonant swing. The capacitor voltage crosses zero only if:

$$V_{\mathrm{DC}} \leq \sqrt{\frac{L_{\mathrm{r}}}{C_r}} I_{\mathrm{L}} \tag{6.14}$$

which is a very strong constraint for sinusoidal inverters. For small load currents, the voltage across the capacitor will not cross zero. The current variation through L_{r} and C_{r} is a cosine function during this time. The moment of time corresponding to zero capacitor voltage is given by:

$$\Delta t_x = \sqrt{L_{\mathrm{r}} C_{\mathrm{r}}} \left[\pi + \arcsin \frac{V_{\mathrm{DC}}}{Z_{\mathrm{r}} I_{\mathrm{o}}} \right] \tag{6.15}$$

After this moment, diode D1 turns on and takes over the L_{r} current and the C_{r} is no longer conducting current. The voltage across the inductor L_{r} is clamped at V_{DC} and its current goes linearly to zero. Throughout this interval of current decrease, the voltage across Sw1 is kept at zero, and any turn-on command produces commutation at zero, voltage after the L_{r} current goes to zero. The time associated with this event is given by:

$$\Delta t_y = \sqrt{L_{\mathrm{r}} C_{\mathrm{r}}} \frac{I_{\mathrm{L}} \sqrt{\frac{L_{\mathrm{r}}}{C_{\mathrm{r}}}}}{V_{\mathrm{DC}}} \sqrt{\left[1 - \left(\frac{V_{\mathrm{DC}}}{I_{\mathrm{L}} \sqrt{\frac{L_{\mathrm{r}}}{C_{\mathrm{r}}}}} \right)^2 \right]} \tag{6.16}$$

The duration of the OFF interval is thus limited by parameters of the resonant circuit:

$$\Delta t_x \leq T_{\mathrm{OFF}} \leq \Delta t_y \tag{6.17}$$

It can be noticed that power semiconductor devices are switched at zero voltage without switching losses. After Sw1 turns on, current through Sw1 increases slowly due to L_{r} under a constant voltage V_{DC}. Diode D2 stays in conduction for another short time interval under the same equivalent circuit derived previously during the D1 conduction. This interval ends when the current through D2 gets to zero. This current equals the difference between the load constant current I_{L} and the linearly increasing current through Sw1.

A complete solution is presented in Figure 6.15 for a three-phase inverter. The capacitors are distributed in parallel with each switch, while the inductance is placed on the DC bus and increased from the value of the parasitic inductance. Modern MOSFET-based inverters can take advantage of the MOSFET's inherent parallel capacitance. After the parasitic inductance is estimated, additional inductance may become necessary to achieve the desired resonant frequency. The resonant frequency influences the voltage swing slope and the delay to zero crossing.

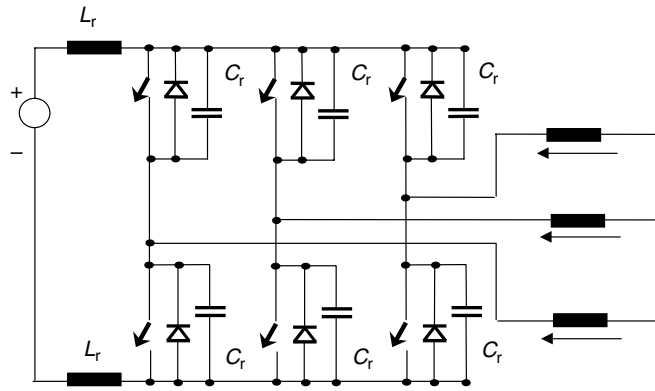

FIGURE 6.15 Distributed resonant snubber.

The early 1990s brought the explosive development of IGBTs and this concept has been widely developed in what we know today as *resonant converters*. A special chapter is later dedicated to this topic.

6.2.5.6 Active Snubbering

Voltage overshoot protection can also be achieved by including an additional stage in the gate driver (Figure 6.16) [11]. At turn-off, the protection transistor Q_p is turned-on and the gate is discharged through it. When the IGBT collector voltage reaches the breakdown voltage of the Zener diode, a current flows through the gate of Q_p and turns it off. The remaining current flows through R_{off}, slowing down the dv/dt rate. An additional benefit of this method is that switching power is reduced by half.

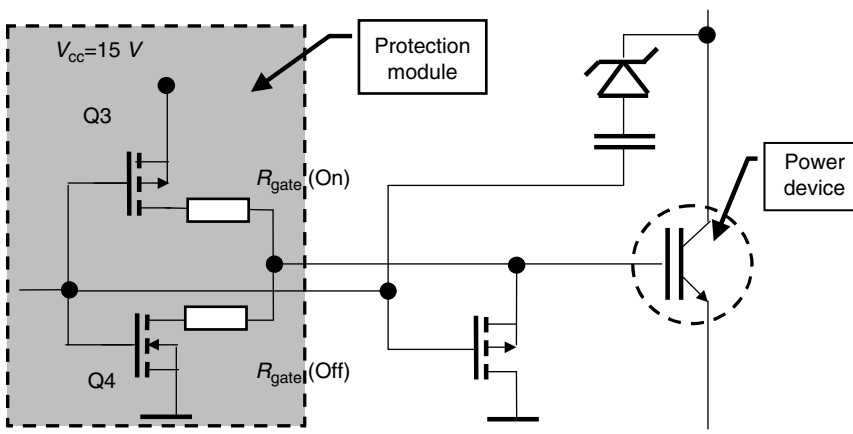

FIGURE 6.16 Active voltage overshoot protection.

6.2.6 Gate Driver Faults

Another possible fault can occur at the gate-driver level. A faulty operation of the gate driver leading to absence of the control pulses at the IGBT gate should be detected and all the six gate drivers of the inverter turned-off. This is generally processed through the control device, an field programmable gate array (FPGA) or a digital signal processor circuit.

6.3 SYSTEM PROTECTION MANAGEMENT

Complex systems including multiple power converters, sources, or loads have a protection system that sets several levels of priority for communication between them. This is discussed in Chapter 11 [12].

6.4 REDUCTION OF COMMON-MODE EMI THROUGH INVERTER TECHNIQUES

Chapter 1 has shown the importance of preventing common- and differential-mode electro-magnetic inference (EMI) in switching power converters and the appropriate standards have been described. Special EMI filters are commercially available for currents up to 100 A in grid-connected applications. They are based on higher order passive filters especially calibrated to limit EMI according to standards.

Let us now take a look at some circuit solutions for the common-mode EMI reduction. Three-phase inverters in which the neutral is not connected experience a continuous variation of the neutral voltage with respect to earth. This is illustrated in Figure 6.17 for a pulse width modulation (PWM) algorithm that represents a sequence of active and zero states already known for the three-phase inverter. Each state of the inverter operation produces a different level of neutral voltage as shown in Table 6.2. The largest neutral voltage change (step) occurs when using zero states. A possible minimization of the common-mode voltage and ground current can be achieved by avoiding zero states within the PWM generation [13,14]. The drawback of such a solution is in increasing the ripple of the motor currents and limiting the maximum modulation index.

The parasitic coupling between the neutral point of the load and ground creates a path for the common-mode current flow. Note that the slope of neutral point voltage variation follows the voltage variation across the power semiconductor switches. The faster are these switchings, the larger is the current to ground. Figure 6.18 shows the capacitor path of the common-mode current.

Capacitor C_g can be the machine's stray capacitance or the distributed parasitic capacitance to ground. These common-mode currents create EMI problems and can produce damage to the electrical machine through bearing current, shaft voltage, insulation breakdown, or current flowing through the stray capacitors between motor and frame. These currents show components within the range of 100 kHz to tens of MHz and cannot completely be removed with ordinary chokes or EMI filters (like *baluns*).

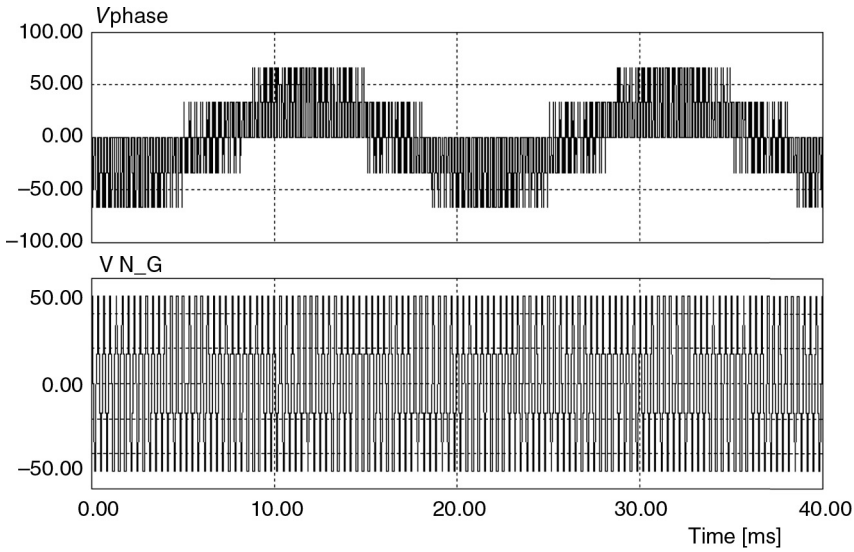

FIGURE 6.17 Variation of the neutral point voltage with respect to the middle point of the DC link for a sinusoidal PWM at 3 kHz and $V_{DC} = 100$ V.

A prior solution considered a common-mode transformer with an additional winding shorted by a resistor (Figure 6.19) [15,16]. The neutral point voltage is detected with an RC three-phase network. In this solution, care has to be taken to choose the appropriate R and C components, as they appear in parallel with each load phase. One improvement is to create the neutral voltage with an iron core transformer that offers very large impedance in parallel with each load phase (Figure 6.19). The resulting current circulates through the fourth winding of a four-winding ferrite-core common-mode inductor [17]. This is used for

TABLE 6.2
Neutral Voltage for Each State of Inverter Operation

[1 0 0]	$-0.16 * V_{DC}$
[1 1 0]	$0.16 * V_{DC}$
[0 1 0]	$-0.16 * V_{DC}$
[0 1 1]	$0.16 * V_{DC}$
[0 0 1]	$-0.16 * V_{DC}$
[1 0 1]	$0.16 * V_{DC}$
[1 1 1]	$0.50 * V_{DC}$
[0 0 0]	$-0.50 * V_{DC}$

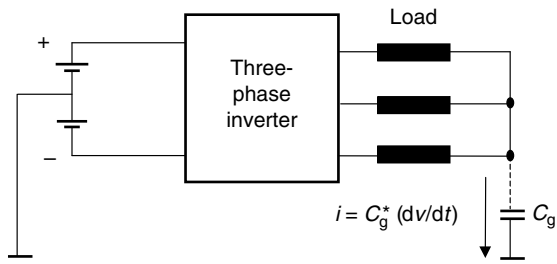

FIGURE 6.18 Common-mode current.

common-mode current cancellation. Furthermore, an RC circuit is used (Figure 6.19) to limit the power dissipation, as only the edges of the common-mode voltage are addressed in order to minimize their slope.

This group of methods has proven inefficient in withdrawing the aperiodic ground-current. Elimination of both oscillatory and aperiodic ground currents (*common-mode voltage*) has been attempted with active circuits [18,19]. They can be used in the horsepower range in which high-frequency transistors are available for common-mode voltage control. One of these solutions is shown in Figure 6.20 [20]. The common-mode voltage at the inverter output is reconstructed with a set of small capacitors C_x and used to control an inverter leg. This adds a compensating voltage at the inverter outputs through the transformer T_r. This completely cancels the common-mode voltage on the load.

The implementation issues of this method relate to the choice of the transistors in the active circuitry. Transistors are operated in the active region following emitters and should have a wide frequency bandwidth and low output impedance to eliminate any influence of the output current in the compensating voltage. The high-frequency bandwidth ensures that the compensating voltage precisely follows the slopes of the inverter output voltages. The power dissipation within

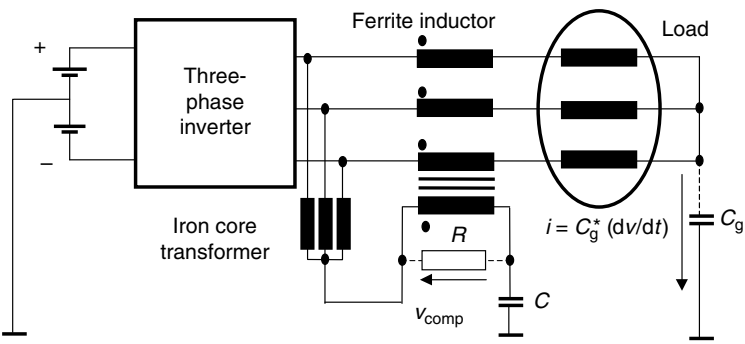

FIGURE 6.19 Common-mode transformer.

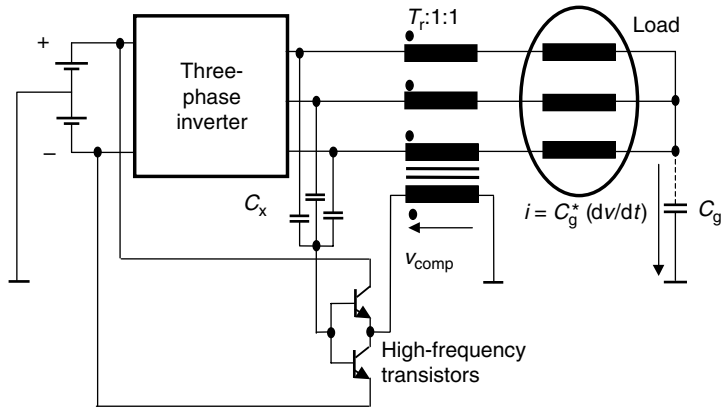

FIGURE 6.20 Active control with high-frequency bandwidth transistors.

these transistors is very small (∼0.5%) as the transistors carry only the transient part of the load voltage.

At high-power levels, none of these approaches based on active common voltage canceling is convenient. The alternative solution consists in using a fourth converter leg. The power converter becomes a converter with four identical legs followed by *LC* low-pass filters. For balanced systems, the fourth leg can be derated with respect to the conventional inverter. The role of this additional leg is to complement the neutral voltage so that the instantaneous sum of all pole voltages is zero and no common-mode current is created. The drawback is that it is not practical to add a fourth load phase for the compensating current. A filter system with four phases can be used to fictitiously create the fourth phase and cancel common-mode voltage at the neutral point. If the load is perfectly symmetrical, this idea works perfectly. It is limited only by the frequency characteristics of the transfer function through the passive components used in filter and load.

Summation of voltage effects is therefore created through the low-pass filters *LC* when the fourth leg voltage is generated by reversing the information from Table 6.2, that is, to have always two switches tied to the positive DC rail and two switches to the negative rail. However, zero states cannot be used within this approach. Other PWM algorithms can however be defined without the use of zero states. A possible solution is to create the effect of zero state by employing two opposite vectors. For instance, if the last active state before the zero state was [1 0 0], we create the effect of the zero state by using the active states [1 0 0] and [0 1 1], each for half of the time desired for the zero state. Figure 6.21 illustrates this principle for a single pulse within the PWM algorithm. The extended time intervals associated with the active states produce more ripple on the load phase currents. In other words, a proper selection of the PWM algorithm can help in reducing the common-mode voltages at the price of increased ripple on the load.

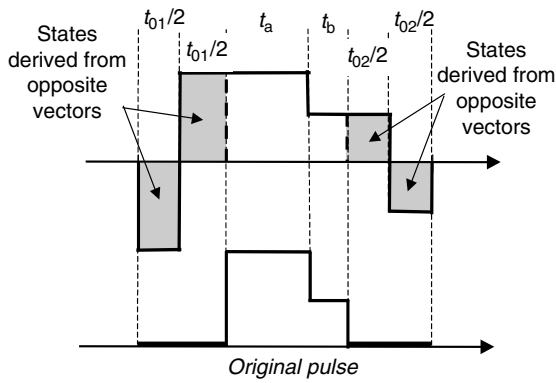

FIGURE 6.21 PWM without zero states.

6.5 TYPICAL BUILDING STRUCTURES OF CONVENTIONAL INVERTERS DEPENDING ON POWER LEVEL

As shown in Chapter 1, the same circuit topology can be used at 10 or 1000 A, but building the appropriate power converters differs with the power level. In order to understand constraints for packaging power converters at different power levels, let us start with a review of power semiconductor packages.

6.5.1 Packages for Power Semiconductor Devices

Figure 6.22 illustrates different packages used for IGBT devices. For currents of tens of amperes through-hole packages, such as TO-220 and TO-247, are preferred for power semiconductor switches. They are used with *printed circuit boards* (PCBs) to build power converters below 40 A. This direction towards use of PCBs has been imposed by power converter manufacturers for cost reasons and to take advantage of the existing PCB-automation tools. These packages benefit from putting both the power semiconductor switch and the associated diode within the same package and offering it at very low cost per ampere. For instance, a 20 A, 400 V IGBT/diode can be found at $1.50 or a 60 A, 600 V IGBT for less than $8.00.

For low- and medium-power applications, IGBTs are packaged in dual (inverter leg) or six-pack assemblies. Unfortunately, the packaging is not consistent from one manufacturer to another and it is similar to the former *bipolar Darlington power modules*.

Modern power modules also include control and protection circuitry within the same package in order to simplify the inverter building and reduce costs of auxiliary parts. There is no standard for these *intelligent power modules* and they are not interchangeable as characteristics, control, or protection. This becomes a serious limitation to paralleling such modules. Single inline package (SIP) and dual inline package (DIP) modules are another alternative for power modules used in low-power appliances.

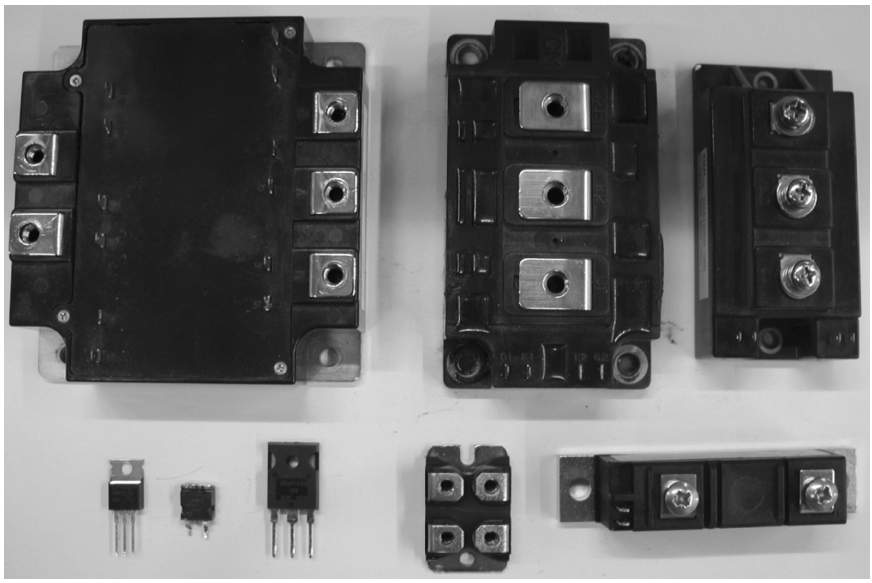

FIGURE 6.22 IGBT packages.

Different manufacturers have tried during the last years to provide standard packages, especially for the low-power market where power converter manufacturing is based on more automation. The EconoPACK (Figure 6.23) and EconoPIM modules are dedicated packages below 20 kW (1200 V, 100 A) and contain a full-bridge with through-hole terminals able to connect the control circuitry from a PCB. Above 100 kW, integrated hybrid modules (IHM) modules are used.

Because a power converter manufacturer generally has to address a wide power range and provide very large volumes at lower power levels, a new approach has won market share during the last few years. The packaging has been changed to accommodate easy paralleling of power modules to define a very large power range that can be easily manufactured. The major features are:

- Define a flow-through concept by separating the power DC terminals on one side and phase output terminals on the other.
- Parallel the three legs of a six-pack IGBT if and when necessary.
- Use the same housing for dies that support currents from 150 to 450 A in order to achieve easy scaling of heatsinks, bus bars, and drivers.

At higher currents, the IGBT modules are mounted directly on heatsinks or cold plates while the electrical terminals are connected through screws on top to special structures called *bus bars*.

In the medium-power range, there is always a temptation to save money by paralleling multiple low-power IGBTs packaged in TO-220 or TO-247 packages.

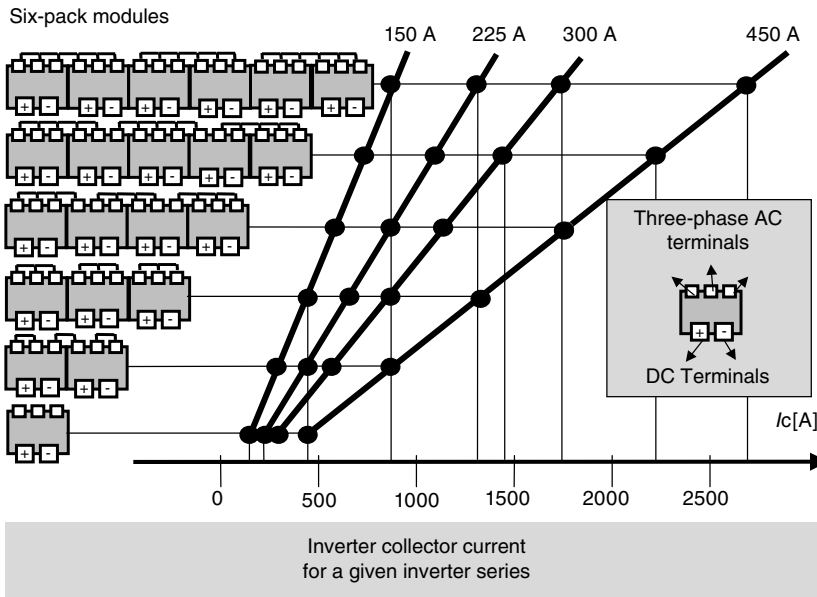

FIGURE 6.23 Packaging for parallel applications: EconoPACK.

However, such an approach loses the advantages of the PCB mounting and requires high-current wiring of all semiconductor power terminals.

All of these higher power modules are more expensive. For instance, a 300 A, 600 V dual IGBT can be purchased for about $240.00; a 600 A, 1200 V dual IGBT for about $300.00; while the largest in family, the 1400 A, 1200 V dual IGBT can be found at $800.00. It is important to understand that the cost of a module is mostly dependent on the mechanical packaging and not on the size of the semiconductor die that is inside. This is why the cost becomes advantageous if the package accomodates the largest semiconductor die that it can.

In the very high-power range, IGBTs are packaged as discrete devices only.

6.5.2 Converter Packaging

Once the power semiconductor devices have been selected and the size and terminals of the appropriate module have been understood, the next element to look at is the converter packaging. It has been mentioned that PCBs are the best solution below 40 A. Multi-layer PCBs allow large currents on different isolated layers. They are suitable for power devices with through-hole terminals.

At higher currents, there are two options for power distribution:

- High current (heavy-gauge) wires: Heavy-gauge wires can be used at reasonable power levels but they introduce difficult routing and bending within the converter enclosure.

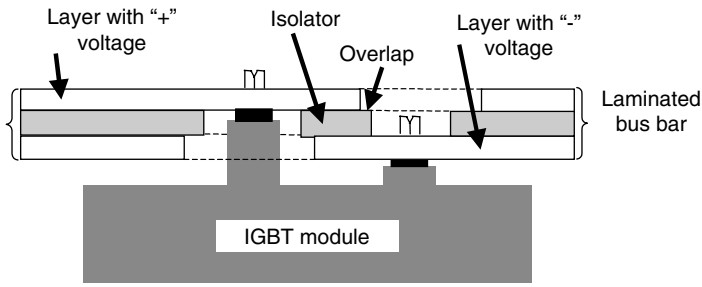

FIGURE 6.24 Possible use of a laminated busbar at IGBT module connection.

- Copper bus bars with tapped holes for cable connection. Copper bus bars are built in different sizes and can carry current in a simple, reliable way. They should be several inches apart from each other and be isolated from the cabinet by fiberglass reinforced plastic spacers.

An alternative solution has been recently introduced that uses laminated bus bars built of a multi-layer structure of copper and dielectric insulator. They were first used in computer and telecommunications systems, but were introduced recently in medium- and high-power converters (Figure 6.24). The advantages of this technology is better cooling, lower resistance than wires (lower voltage drop), minimized stray inductance (lower voltage overshoots), and the possibility to use different copper layers in the laminated package for different purposes. For instance, a direct comparison of a connection with twisted wires and one with a laminated bus bar shows half DC resistance of the new solution (0.006 versus 0.0032 Ω), and a substantial decrease in the high-frequency impedance at 1 MHz from 0.078 to 0.019 Ω. Using each layer for another function highly improves packaging of power converters for modern requirements up to 1000 A or 5000 V [21].

Due to their ruggedness, they can also be used as mounting platforms for auxiliary components, such as protection circuitry breakers or snubbers [21,22]. Moreover, special structures are built for IGBT devices or modules to accommodate their terminals (Figure 6.24).

6.6 THERMAL MANAGEMENT

The most important criterion in packaging consists of thermal management. All power semiconductors dissipate their switching and conduction losses and these should be removed as fast as possible. As this power is mainly removed through a contact surface with a cooling system, the whole size of the power converter and the power density within the equipment depend on the quality of the thermal transfer through the selected cooling system. Modern power converters expect a power removal of up to $200-500\,\mathrm{W/cm^2}$ — that represents about half of the mean power density of the sun's surface.

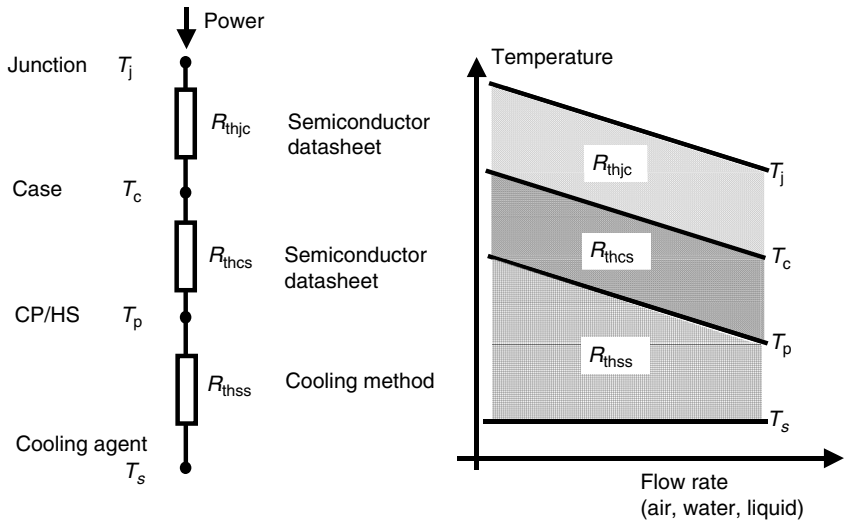

FIGURE 6.25 Equivalent model of a thermal system for a semiconductor device.

A model for a typical thermal circuit is presented in Figure 6.25 and the change in temperature from the junction to the cooling agent ($T_j - T_s$) under a given power dissipation P is provided by the following relationship:

$$T_j - T_s = P\left[R_{thjc} + R_{thcs+thss}\right] \tag{6.18}$$

where R_{thjc} represents the junction-to-case thermal resistance, R_{thcs} represents the case-to-cooling thermal resistance and R_{thss} represents the thermal resistance of the cooling system from the cooling agent (air, water, liquid) to the surface. It is, therefore, obvious that a lower equivalent resistance will keep the junction closer to the temperature of the cooling agent. The first two terms are provided by the semiconductor device datasheet and they are the same for a given device. The only solution here is to go to higher ratings in order to minimize the thermal resistance. The last term in Equation (6.10) corresponds to the cooling system, and that depends on the method chosen, the cooling agent, the material and shape of the heatsink or cold plate, the flow rate of the cooling agent, and so on. Let us analyze the options we have.

Figure 6.25 shows that the higher the flow rate, the smaller the thermal resistance and the better the cooling. However, the cooling device itself and the connecting pipes limit the flow rate of the cooling agent. Secondly, let us note the multitude of choices for cooling systems and their selection depends on the system requirements and cost (Figure 6.26) [23].

Once the method has been selected, the type of cold plate or heat sink is the next area of focus. Different materials like aluminum or copper are used in manufacturing and their shapes can be different to facilitate the easy transfer of thermal energy. Materials and shapes of thermal devices able to handle these requirements are

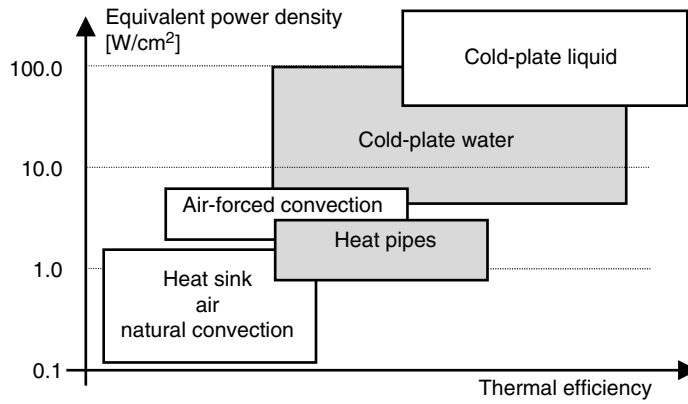

FIGURE 6.26 Thermal efficiency of different methods used for cooling.

designed and selected based on knowledge of physical laws of thermal conduction, thermal radiation, nature of forced convection or phase convection. The final criterion here is the cost of the device, as a more complex mechanical structure able to remove more heat will also cost more.

The cooling agent can be air, water, or a special agent with a larger heat capacity. For example, removing the same power dissipation of 244 W from a three-phase converter produces an increase of 40°C on an air-cooled heat sink and only 2.8°C rise in a water-cooled system [22]. Liquids with better heat capacity are based on different glycol solutions [24].

6.6.1 Transient Thermal Impedance

All the previous analyses have focused on steady-state thermal aspects when the average loss of power is known. In many applications, power semiconductor devices are stressed by transient overcurrents with large instantaneous dissipation. Modeling transient thermal impedance requires definition of a new parameter, *heat capacity*. This represents the rate of change of the heat energy with respect to the material temperature. The heat capacity per volume yields:

$$\frac{dQ}{dT} = C_v$$

The transient behavior of the junction temperature is related to the time-dependent heat diffusion equation with a simplified solution given by the analog-equivalent circuit shown in Figure 6.27. The equivalent of the heat capacity is a capacitor able to slow down the junction temperature variation when a step change in power is applied.

Identical to the analog circuitry, a thermal time constant can be defined as:

$$\tau_{th} = \frac{\pi}{4} R_{th} C_{th} \tag{6.19}$$

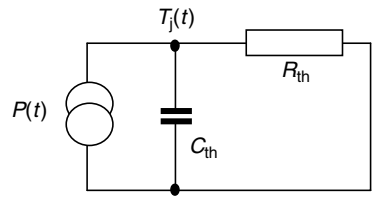

FIGURE 6.27 Transient thermal model.

Packaging materials and structures are always designed to minimize the thermal resistance as the loss power is transferred usually *in average*. For this reason, the thermal time constant as well as the power transient capability of a device are limited. However, it has been proven that power semiconductor devices can withstand large overload capabilities that exceed their average power ratings.

Completing Figure 6.25 with the transient model yields the equivalent circuit shown in Figure 6.28. The temperature evolution in time and space when a pulse power is applied is also shown.

Transient thermal models are very useful in thermal analysis of power converters switched at high frequency with a variable duty cycle. The cooling system should sustain pulses of power with considerable thermal dynamics.

6.7 CONCLUSION

This chapter presents details related to the building of a three-phase power converter. Information about three-phase power converters can easily be found in many

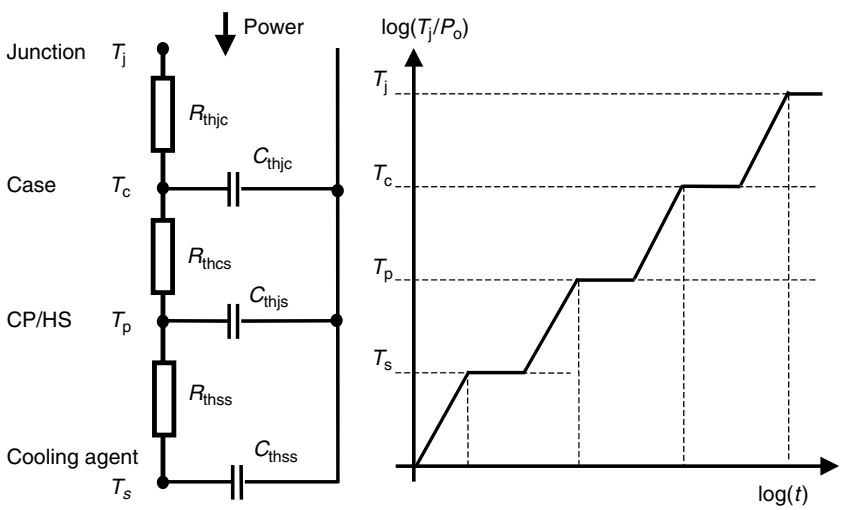

FIGURE 6.28 Transient equivalent circuit and temperature evolution in time.

textbooks, but the way the converter is built and protected is also important. Modern techniques have been shown to improve performance criteria such as efficiency, power density, and input or output harmonics.

6.8 PROBLEMS

P.6.1 A 24/120 V boost converter is built with an IGBT and a diode switched at 20 kHz. The IGBT is protected with a snubber capacitor. The parasitic inductance of the circuit is 10 nH, the maximum input current is 100 A, and a voltage increase of maximum 5% is allowed. Estimate the required snubber capacitance.

P.6.2 Select a resistor to form an RC snubber circuit for the previous converter. Calculate losses within the resistor.

P.6.3 Consider a single-phase IGBT inverter with snubber circuits across each IGBT. The DC voltage is 270 V, switching frequency is 16 kHz, maximum current is 120 A, and a voltage overshoot of 10% is allowed. The bus parasitic inductance has been estimated at 20 nH. Define the values for the resistor and capacitor and estimate resistor power losses.

P.6.4 Explain how an RC network connected in parallel with the load would serve as a turn-off snubber for all four IGBTs in the previous problem. Calculate values of components within such a network and estimate power losses. Why is the solution of the previous problem preferable?

P.6.5 Rewrite the space vector modulation time equations for Figure 6.29.

P.6.6 Common-mode current is produced by the derivative of neutral voltage. This current is lower for PWM algorithms that do not produce large variations of the neutral point voltage. Considering Table 6.1 along with the switching sequences

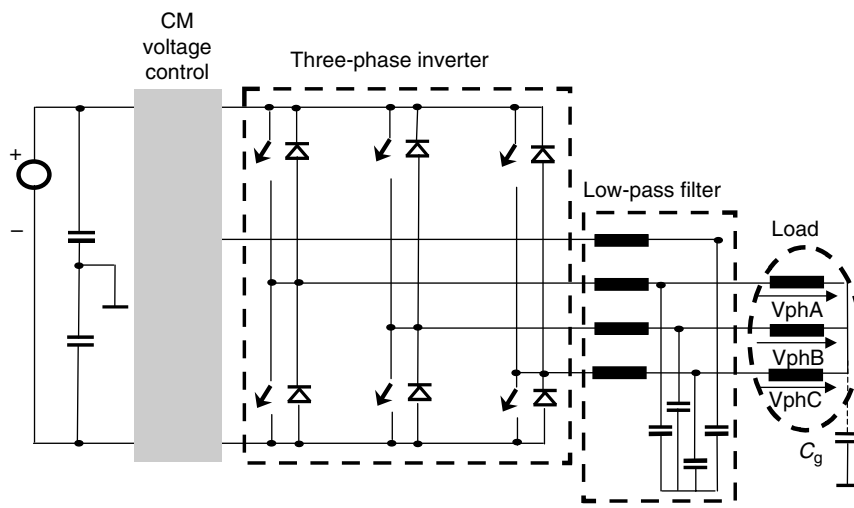

FIGURE 6.29 Four leg inverter.

considered in the previous chapter for SVM algorithms, determine which state sequence produces the lowest peak-to-peak common-mode current.

P.6.7 Draw for each sequence the qualitative evolution of the common-mode current. What is the frequency of the most important component?

P.6.8 A buck converter built with an IGBT and a diode is switched at a frequency f_{sw} with a constant duty cycle producing an ON-state loss of 100 W and a switching loss of $0.01 * f_{sw}$. The maximum junction temperature of the IGBT is 150°C and the junction-to-case thermal resistance is 2°C/W. The cooling system maintains a quasi-constant case temperature at 60°C. What is the maximum allowable switching frequency?

P.6.9 Consider the same IGBT mounted on a heatsink while the ambient temperature is 27°C. Consider a switching frequency of 16 kHz and calculate what is the maximum heatsink thermal resistance.

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