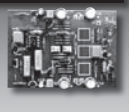


A Phono PrePreamp for the (SA) CD Age, Part 2

By Norm Thagard

With design considerations and components selection covered in the first part of this series, we now proceed to the design specifics for the moving-coil preamplifier.

Figure 3 shows the moving-coil preamplifier schematic. Beginning at the input side of the circuit, note that the RCA input jack should be insulated from the chassis and the ground terminal of the jack bypassed to the chassis via a 10nF capacitor that is labeled C_{rf}. This avoids a potential ground loop while bypassing the ground terminal to chassis to suppress RF that might otherwise enter the circuit via the cable shield. C_{rf} can be a ceramic capacitor.

CIRCUIT COMPONENTS

The resistor labeled R_{in} sets the input resistance of the preamplifier. Its value should be equal to the load resistance recommended by the cartridge manufacturer for input into a "head amp." For the prototype, the value used was 100Ω based on the cartridge manufacturer's recommendation. Some designers provide an array of input resistors with DIP switch selection of the recommended value.

My approach was to solder two gold-plated pins removed from a good-quality DIP IC socket into the PC board. These pins readily accept the leads of a ¼W precision resistor whose value is that recommended by the cartridge manufacturer. Should a new cartridge require a different resistor value, it is a simple matter to pull the old resistor from the pins and insert the new resistor.

I used no input capacitor, because I believe that moving-coil cartridges are relatively insensitive to capacitive loading. Neither Audio-Technica for their OC9/MLII nor Shelter for its 501, for example, specify a particular capacitance loading for these two cartridges.

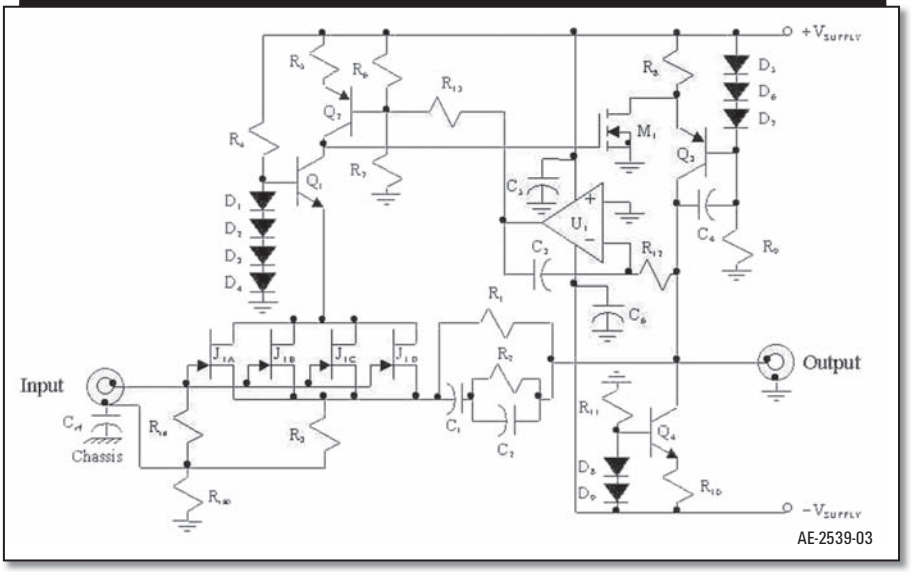
R_{iso} was added based on a suggestion in *The Art of Electronics*[19]. It lets the phono cartridge ground lead set the potential at that node, reducing (you hope) the effect of noise on the preamp ground bus. Any noise coming in on that lead appears unamplified at the output while cartridge output is amplified by the rather large closed-loop gain of the phono preamp, yielding a "pseudo-differential input configuration." With one exception, I saw no objective change in preamp performance with or without R_{iso}, so if its presence offends a builder's sensibilities, by all means delete it.

A typical 2SK170 JFET will have about 45pF input capacitance, so four of them would present almost 200pF to the cartridge in the absence of Miller effect. J_{1A} – J_{1D} constitute the common source (CS) portion of a cascode, which minimizes but does not, as some texts claim, eliminate Miller effect. Miller capacitance here would be $C_{Miller} = 4C_{gd}(1 - a)$, where $C_{gd} \cong 20$pF is a typical value for gate-to-drain capacitance in a 2SK170 JFET. In this preamplifier, CS gain is $a = -g_{m\text{-}JFETs}/g_{m\text{-}Q3} < -1$ because the tranconductance $g_{m\text{-}Q1}$ of bipolar junction transistor (BJT) Q_1 is approximately 1S*, while the combined transconductance of J_{1A} – J_{1D} is perhaps a little more than 150mS.

Although the 2SK170 has relatively high transconductance for a JFET, it is nonetheless significantly lower than a similarly operated BJT. The upshot is that C_{Miller} is slightly greater than $4C_{gd}$ or about 100pF. To this must be added $4C_{gs} \cong 100$ pF. Note that although the intrinsic gate-to-source capacitance is slightly greater than the intrinsic gate-to-drain capacitance, the latter potentially contributes more to the input capacitance of the preamplifier due to Miller effect.

Based on the reasoning in the previous two paragraphs, if a cartridge

FIGURE 3: Moving-coil preamplifier schematic.



requires significantly less than 200pF capacitive loading, then it would seem to be incompatible with this preamplifier. However, the input impedance is more complicated than this due to global negative feedback, which I have neglected due to its analytical complexity. You could sacrifice noise performance for reduced input capacitance by eliminating one or more of J_{1A} – J_{1D}, but noise performance is very important in the first stage of a gain-of-10,000 preamplifier.

If the cartridge requires more than 200pF, simply add an extrinsic capacitor C_{in} in parallel with R_{in} so that C_{in} + 200pF = recommended capacitive load. I hope that any capacitive loading requirement is a loose one because the previous calculations, while theoretically sound, are based on typical values for JFET parameters. Actual values can sometimes vary greatly from the typical.

PSPICE

In this preamp, quiescent drain current I_{DQ} for the input JFETs is set by the DC voltage drop across R_3. Assuming matched JFETs, then $V_{GSQ} = -4I_{DQ}R_3$. The JFETs are therefore self-biased and will assume a value of I_{DQ} that is a function of their intrinsic parameters I_{DSS} and V_P according to the square-law equation $I_{DQ} = I_{DSS}(1 - 4I_{DQ}R_3/V_P)^2$.

I think it's difficult in the new millennium to be a serious designer without a working knowledge of PSpice. It might be illustrative, then, to look at how the simulation program deals with JFET bias. JFET models in PSpice directly use pinch-off voltage V_P, although it is called the threshold voltage and symbolized as VTO. While I_{DSS} is not directly specified, it can be determined from I_{DSS} = VTO^{2*}BETA, where BETA is a PSpice parameter with units of A/V^2 called the transconductance coefficient.

The PSpice model for the 2SK170 has VTO = V_P = –0.5024 V and BETA = 0.05986 A/V^2, so I_{DSS} = VTO^{2}BETA = (0.5024)(0.05986) = 15.11mA. To complicate matters, the intrinsic JFET model with these values of V_P and I_{DSS} is augmented by a series source resistance RS = 4.151Ω that will increase $|V_{GS}|$ by $I_D \times$ RS. This slightly increases the complexity of the square-law equation, but even so JFET bias drain current in PSpice for the input stage can be predicted from **Equation 1**.

Numerically: I^2_{DQ}–0.0702I_{DQ} + 0.000433 = 0. From the quadratic formula in **Equation 2**, you can immediately rule out the former result because it is much greater than I_{DSS}. PSpice therefore should, if our calculations are correct, yield a drain current of 6.83mA. However, the simulation value was 6.86mA, a discrepancy that might be thought to be due to rounding error, but is not.

In real FETs, I_{DQ} will be increased above the square law value by a factor 1 + λV_{DSQ}, where λ is the channel-length modulation. PSpice accounts for this with the parameter LAMBDA, which for the 2SK170 is 0.001923V^{-1}. The effect of LAMBDA is analogous to the Early effect in BJTs. In fact, Early voltage, designated by V_A, is analogous to 1/λ. In the saturation region, drain current will increase linearly with increasing drain-source voltage, exactly as though there were an intrinsic resistor r_d from drain to source. This resistance, sometimes designated r_o in textbooks, is determined by triangle relationships on the i_D – v_{DS} graph to be 1/(λI_D), where I_D is the drain current calculated from the square-law equation neglecting the effect of channel modulation. In the present example, r_d = 1/[(0.001923)(0.00683) ≅ 76kΩ.

In general, intrinsic collector-emitter resistance in BJTs is lower than r_d. The result is that in their respective normal operating regions, FET i_D – v_{DS} curves are "flatter" than BJT i_C – v_{CE} curves, i.e., an FET more ideally, which is to say more closely behaves like a pure transconductance device (voltage-controlled current source).

Using V_{DSQ} = 1.47V from the simulation to adjust the above result gives I_{DQ} = 6.85mA. The above result indicates that while addition of r_d to the JFET model improves its fidelity, drain current errors are minor if this resistance is omitted. There is also a drain ohmic (contact) resistance denoted RD which would change V_{DSQ} by a few tens of mV and affect the result even less than the omission of r_o.

In point of fact, the typical values

in the manufacturer-provided PSpice model may be vastly different than those for the actual physical device the builder has in hand. In the case of 2SK170s, the manufacturer presorts them into three I_{DSS} groups. This is convenient for the builder since the parameter spread is reduced. Unfortunately, a given distributor may not have the group that would be wanted for a given design. I matched JFETs on a curve-tracer for I_{DSS} = 12mA and $I_{DQ} \cong$ 6mA was observed for $J_{1A} - J_{1D}$.

On a closing note, it not only is possible to display PSpice device parameters, it is possible to alter them. Thus, knowing that my 2SK170 parameters differed from the PSpice model values, it was easy to edit the "instance" (simulation) values to correspond to the actual values in order to force the simulation to behave more like the real circuit.

This is as far as we'll explore this topic here. I could not resist the temptation to expand the topic, but this author cannot—nor would the editor tolerate coverage of all of analog electronics in one article.

CIRCUIT OPERATION

I mentioned previously that the input stage topology is BiFET cascode with JFETs in the CS portion. If, as transistors are added in parallel, the total drain current is maintained constant, then g_m increases and hence improves voltage noise performance by the factor $\sqrt{N}$, where N is the number of paralleled devices.

No source resistors are used for $J_{1A} - J_{1D}$. While this avoids the degradation in noise performance that would accompany the resistors, it also removes the negative feedback that would tend to equalize drain currents among the four devices. Therefore, matching of JFETs is recommended and is not difficult to do, even without a curve tracer[20]. After matching, I verified that in-circuit I_D between devices differed by no more than 10%, even after extended operation.

The only way to achieve the necessary open-loop gain is to use active loads. Q_2 and R_5–R_7 form an active load for the first stage cascode. The R_6R_7 voltage divider sets Q_2 base voltage. Q_2 emitter voltage will be about 0.7V higher and $R_5 = V_{R5}/I_{R5} \cong V_{R5}/(I_{DQ}-J_{1A} + I_{DQ}-J_{1B} + I_{DQ}-J_{1C} + I_{DQ}-J_{1D}) \cong (V_+ - V_{EQ-Q2})/(4I_{DQ-J1A}) = \{[R_6/(R_6 + R_7)]V_+ - V_F]\}/(4I_{DQ-J1A})$, where $V_F = -V_{BEQ-Q2} \cong 0.7V$. The subscript "$_Q$" in, e.g., V_{EQ}, implies that it is the "quiescent" or DC bias value of the parameter that is specified.

In the present case, $I_{R5} \cong 4I_{DQ-J1A} \cong 24mA$, *i.e.*, I_{R5} is determined by the combined drain current of the self-biased JFETs. Increasing R_5 will reduce shot noise from the active load via increased degeneration[21] (local negative feedback) but will also simultaneously move Q_2 closer to saturation, a condition that will occur when emitter voltage falls to within 0.3V or so of the fixed collector voltage. Global negative feedback will set MOSFET $M1$'s gate voltage as required, which in turn will fix Q_2 collector voltage to a level as high as 4V. If the value of R_5 is constrained to keep $V_{EQ-Q2} \geq (V_{CQ}-_{Q2})_{max} + 1V \cong 5V$, then $V_{CEQ-Q2} \geq 1V$, guaranteeing active region operation. This means that R_5 should not drop more than $V_+ - 5V = 13V \Rightarrow R_5 \leq [18 - (4.3 + 0.7)/0.024] = 542\Omega$.

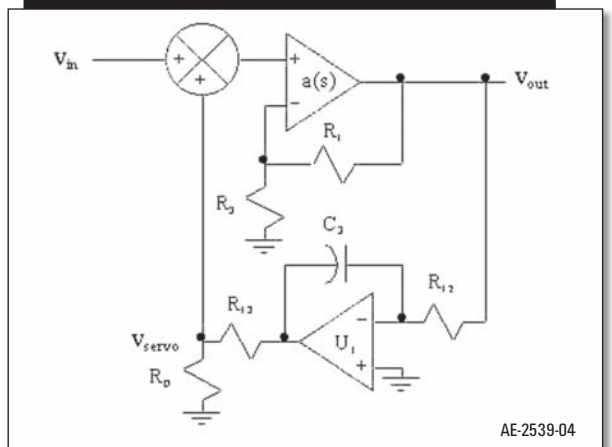
If V_{EQ-Q2} = 5V, then $V_{BQ-Q2} \cong$ 5V – 0.7V = 4.3V. The R_6R_7 voltage divider sets V_{BQ-Q2} according to **Equation 3**.

While this consideration dictates the R_6/R_7 ratio, it does not constrain their absolute values. Reducing the value of $R_6||R_7$ will reduce the active load noise contribution and, as you will see, lower the DC servo cutoff frequency, which is desirable. However, the "stiffer," i.e., more constant, voltage division may make it impossible for the current-limited servo to adjust Q_2 base voltage sufficiently to maintain the output quiescent voltage at zero. Another negative aspect of the stiffer voltage divider is increased power consumption. Reducing $R_6||R_7$ below approximately 350Ω gave negligible improvement in noise level and it was unnecessary to do so in order to maintain low-frequency RIAA curve tracking.

By adjusting base voltage of current-source transistor Q_2, the inverting integrator of subcircuit $U_1C_3R_{12}R_{13}$ controls Q_2 conductivity. Since V_{EQ-Q2} is fixed, this means that the servo will adjust Q_2 collector voltage and hence M_1 drain current to that required to null quiescent output voltage.

This may sound a bit complicated, but a couple of points should help. First, drain and collector currents in active region transistors are to a first order approximation set by—and only by—gate-source and base-emitter voltages, respectively, according to a square-law equation for FETs and the exponential Ebers-Moll equation for BJTs. Second, avoid use of either of these equations in design work if at all possible. This is usually possible because the transistor equations must simultaneously be compatible with the circuit equations à la the old tube load lines. Simplest design is therefore accomplished by having the circuit equations dictate transistor behavior.

FIGURE 4: Simplified DC servo configuration.



Equation 1.

$$I_{DQ} = I_{DSS}\left(1 - \frac{-(4R_3 + RS)I_{DQ}}{V_P}\right)^2 \Rightarrow I_{DQ}^2 + \left(\frac{2V_P}{4R_3 + RS} - \frac{V_P^2}{(4R_3 + RS)^2 I_{DSS}}\right)I_{DQ} + \frac{V_P^2}{(4R_3 + RS)^2} = 0.$$

Equation 2.

$$I_{DQ} = \frac{-(-0.0702) \pm \sqrt{(-0.0702)^2 - 4(1)(0.000433)}}{2} = 0.0351 \pm 0.5\sqrt{0.0032} = 0.0351 \pm 0.0283 = 63 \text{ mA or } 6.83 \text{ mA}.$$

I typically design using Kirchhoff's voltage and current laws in circuits that force desired transistor behavior. Negative feedback helps, too. In fact, use of active loads as is done here is only possible with either DC feedback or servo control. Otherwise, there is nothing to force the transistors to assume the proper bias conditions.

Finally, analyze the prospective behavior of your circuit under the assumption that the transistors are in their active regions unless a given transistor is intentionally to be in cutoff or saturation (ohmic or triode region in the case of FETs). Your analysis will lead to certain voltage and current conditions that should be compatible with active region operation. If these voltages and/or currents are not so compatible over the possible range of transistor parameters, locate the problem and try again.

DC SERVO DESIGN

I have designed several DC amplifiers. It would be nice if this phono preamp could respond to DC, but even a differential design would have problems maintaining the desired bias stability in this case. Perhaps some elaborate thermal compensation scheme would provide the necessary stability. Alternatively, an AC-coupled design could ease the problem, but this would place capacitors in the signal path, which seems to be a no-no in high-end designs. Also, the use of active loads requires DC feedback to maintain the bias point.

A DC servo offers an attractive method for bias point stability while avoiding coupling capacitors. As I will show, however, such a servo will pose design problems in its own right. The major problems are achieving a sufficiently low cutoff frequency so as not to affect low-frequency RIAA curve tracking while maintaining sufficient control range. Fortunately, these are surmountable as the current design proves.

But for an article in *TAA*[22], I might never have begun using DC servos. The article offered without derivation the design equations. The phono preamp is noninverting as is the signal path from Q_2 base to the output. From this it follows that for application of low-frequency negative feedback the appropriate servo configuration is that of a noninverting amplifier with an inverting integrator. I therefore offer the derivation for component values for the configuration in **Fig. 4**.

The schematic is overly simplified in that gain v_{out}/v_{in} is greater than gain v_{out}/v_{servo}. This occurs because inputs at the base of Q_2 and the gates of J_{1A} – J_{1D} are amplified by what is shown in **Equation 4**, respectively, where R_L is the effective resistance at the node common to the collectors of Q_1 and Q_2. It should be recognized that the formulae above are those for CE or CS stage gain in the presence of emitter or source degeneration, respectively. Even though the JFETs constitute the CS portion of a BiFET cascode, the gain expression is identical to that for a CS stage with drain load resistance R_L.

Since gain from this node to the output is the same for either input, the ratio of open-loop gains between the two signal paths is:

$$\frac{a_{J_{1A}-J_{1D}}}{a_{Q2}} = \frac{1/g_{m,Q2}+R_5}{1/g_{m,J_{1A}-J_{1D}}+R_3} \quad .$$

Although transconductance of Q_2 has already been noted to be several times that of the combined transconductance of J_{1A} – J_{1D}, $R_5 >> R_3$ nonetheless results in $v_{out}/v_{in} > v_{out}/v_{servo}$ as asserted. In fact, the ratio of gains is roughly 30 so local feedback provided by emitter degeneration resistor R_5 eases the difficulty of lowering the servo cutoff

Equation 3.

$$V_{BQ-Q2} = \frac{R_7}{R_6+R_7}V_+ = 4.3\text{V} \Rightarrow \frac{R_7}{R_6+R_7} = \frac{4.3\text{V}}{18\text{V}} = 0.239 \Rightarrow R_7 = 0.314R_6.$$

Equation 4.

$$a_{Q2} = \frac{R_L}{1/g_{m,Q2}+R_5} \quad and \quad a_{J_{1A}-J_{1D}} = -\frac{R_L}{1/g_{m,J_{1A}-J_{1D}}+R_3},$$

frequency. This need not be accounted for separately since the same effect could be obtained by reducing v_{servo} by a change in the voltage division provided by $R_D R_{13}$.

The **Fig. 3** schematic component designations have been retained for ease of understanding the servo configuration that is actually operative in this phono preamplifier. The summing junction provides negative feedback due to the sign reversal provided by the inverting integrator. R_D is the parallel combination of $(\beta_{Q2} + 1)(R_5 + r_{e\text{-}Q2})$, R_6, and R_7, which is approximately $R6||R7$. The bottom terminal of the summing junction represents the Q_2 base. It is not necessary to know what a(s) is, except that its magnitude at any frequency of interest should be and is very high.

Only R_1 and R_3 are shown in the preamp's feedback loop because the servo, if properly designed, will be unable to respond to audio frequency stimulus. Thus, we are interested only in the low-frequency gain $A_0 = 1 + R_1/R_3 \cong 10{,}000$.

Noninverting terminal voltage is the output from the summing junction, which is:

$$v_+ = v_{in} + [R_D/(R_D + R_{13})]v_{int},$$

where $v_{int} = -[1/(sR_{12}C_3)]v_{out}$
is the output voltage of the integrator. In turn: $v_{out} = (1 + R_1/R_3)v_+ \Rightarrow v_+ = v_{out}/(1 + R_1/R_3)$.

Therefore: see **Equation 5**.
Grouping terms: see **Equation 6**.

Substituting $j\omega$ for s in the above expression, the gain v_{out}/v_{in} is found to be that shown in **Equation 7**.

Gain magnitude is $|A_V(jf)| = (1 + R_1/R_3)/[1 + (f_o/f)^2]^{1/2}$. From this, it follows that $|A_V(j0)| = 0$, $|A_V(jf_o)| = (1 + R_1/R_3)/(2^{1/2})$, and for $f >> f_o$, $|A_V(jf)| \cong 1 + R_1/R_3 = A_0$.

These results imply the existence of a zero at DC and a pole at f_o. Of course, $|A_V(jf)|$ actually tracks the RIAA curve, so these results merely manifest the simplifying assumption made at the outset. The integrator will have no noticeable effect on circuit operation for frequencies much greater than f_o. To preclude deviations from the RIAA curve due to the servo, it is necessary to ensure that $f_o << 20Hz$.

GOOD NEWS, BAD NEWS

The gain equation describes a high-pass filter with cutoff frequency f_o, so the servo does not allow the preamplifier to respond to DC. Although the gain expression may, at first glance, look a little complex, closer examination reveals that the integrator time constant $R_{12}C_3$ will be divided by DC closed-loop gain $1 + R_1/R_3$ and by the voltage divider ratio $R_D/(R_D + R_{13})$ at the integrator output.

The integrator time constant should be as large as practical. To avoid use of electrolytic capacitors, it seems reasonable to restrict the value of C_3 to no more than 10µF. Op amp U_1 is a JFET-input op amp that should work well if $R_{12} = 1M\Omega$. The fundamental cutoff frequency due to the integrator would be $1/(2\pi R_{12}C_3)$ = 0.016Hz. This is great, but the bad news is that it is multiplied by the low-frequency closed-loop gain of the preamplifier, which is A_0 = 10,000.

The good news is that the voltage divider formed by $R_D R_{13}$ can potentially salvage the situation. However, there are confounding considerations for this divider. Resistance R_D must be as small as possible, but smaller values increase power consumption and lower the offset range over which U_1 can maintain null output. There is an upper limit on resistance values as well if Q_2 base bias current requirements are to be met. As mentioned, local feedback from R_5 has the same effect as lowering the voltage divider ratio, which eases the constraint on the divider. Ain't electronics wonderful!

Due to this bonus effect of R_5, the time constant $1/(2\pi R_{12}C_3)$ can be ten times greater without compromising the low-frequency cutoff. The obvious thing to do, then, is to choose a smaller value for C_3 because a good-quality 1µF capacitor is much smaller, cheaper, and more widely available than one of 10µF value. The fact that the preamp tracks the RIAA curve with 0.1dB accuracy down to 20Hz with output offset voltage of approximately 1mV proves that the servo does its job.

The values used in the R_6R_7 voltage divider worked fine for JFETs with I_{DSS} = 12mA. Should I_{DSS} be significantly greater than this, then the divider ratio should be modified to lower Q_2 base voltage. Of course, if I_{DSS} is significantly less than 12mA, then base voltage should be increased. Alternatively, R_5 could be reduced in the former or increased in the latter case. A decrease in the value of R_5 could, however, affect RIAA tracking at low frequency.

As a matter of interest, you could use a zener diode in lieu of R_6 or R_7, taking advantage of the diode's low dynamic impedance, which can be about 2Ω for a 1N4735 operated at 41mA[23]. The disadvantage is that the ability of the servo to null output would be restricted to an impracticably small offset range. Placing a small resistor in series with the diode would loosen this restriction and reduce the noise contribution of the zener (zeners can be very noisy) but would also partially nullify the benefit of using the zener in the first place. Even with the resistive divider, it may be necessary to alter either the value of R_5 or the R_6/R_7 ratio should the JFET drain currents differ significantly from those obtained in the prototypes, as mentioned in the previous paragraph. In fact, the values offered here seemed to be variable over quite a range while still giving normal operation.

As a final note, you could add a capacitor shunting R_6 to reduce noise at middle and high audio frequencies. Perhaps it should be added to increase

Equation 5.

$$\frac{v_{out}}{1+R_1/R_3} = \frac{R_D}{R_D+R_{13}}\frac{-1}{sR_{12}C_3}v_{out} + v_{in} \Rightarrow v_{out} = -\frac{R_D}{R_D+R_{13}}\frac{1+R_1/R_3}{sR_{12}C_3}v_{out} + \left(1+R_1/R_3\right)v_{in}$$

Equation 6.

$$v_{out}\left(1+\frac{R_D}{R_D+R_{13}}\frac{1+R_1/R_3}{sR_{12}C_3}\right) = v_{in}\left(1+R_1/R_3\right)$$

Equation 7.

$$A_V \equiv \frac{v_{out}}{v_{in}} = \frac{1+R_1/R_3}{1+\dfrac{R_D}{R_D+R_{13}}\dfrac{1+R_1/R_3}{j\omega R_{12}C_3}} = \frac{1+R_1/R_3}{1-j\,f_o/f}, \text{ where } f_o = \frac{1}{2\pi R_{12}C_3}\left[\left(1+R_1/R_3\right)\frac{R_D}{R_D+R_{13}}\right]$$

power supply rejection, because variations in the positive power supply are otherwise amplified. Unfortunately, the capacitor would provide little benefit at low frequency where JFET flicker noise dominates and will produce instability in servo operation unless a zero is introduced into the integrator[24]. I chose the alternative of a fairly elaborately filtered and regulated low-noise positive power supply.

CONSTANT–CURRENT SOURCES

There are two constant-current sources in this preamplifier, both serving as active loads. As we just saw, the current source formed by Q_2 serves the additional role of completing the DC servo loop. Its emitter resistor R_5 enhances performance by increasing the Norton-equivalent resistance of the source from r_{o-Q2}, which is the intrinsic collector-emitter resistance of Q_2, to $(1 + g_{m-Q2}R_5)\ r_{o-Q2}$. Current-source current will be $\{[R_6/(R_6 + R_7)]V_+ + V_{BE-Q2}\}/R_5 \cong \{[1{,}000/(1{,}000 + 866)]18 + (-0.7)\}/392 = 23mA$, anticipating that $J_{1A} - J_{1D}$ will require a total of 20–25mA. As discussed previously, current-source current will be modulated by the servo to set Q_3 emitter current at the level needed to maintain output offset voltage near zero.

The second stage is a folded-cascode whose current source/active load consists of $Q_4D_8D_9R_{10}R_{11}$. It will command Q_4 collector current of $(V_{D8} + V_{D9} - V_{BE-Q4})/R_{10} \cong 0.7/18.2 = 38.5mA$. While this current command does not directly set Q_3 collector current, it will indirectly do so. Always keep in mind that active region transistor collector or drain current is set by base-emitter or gate-source voltage, respectively.

DC feedback via the servo is the key as it sets M_1 gate voltage and hence MOSFET quiescent drain current to that value necessary to null output quiescent voltage. It accomplishes this by adjusting the emitter voltage of Q_3 through the resulting R_8 voltage drop. This voltage drop is produced by current through R_8, which will be $(V_{D5} + V_{D6} + V_{D7} + V_{BE-Q4})/R_8 \cong 1.4/15.0 = 93mA$, of which about half will flow into the emitter of Q_3 and half into the drain of M_1. These bias currents were set, by the way, on the basis of the minimum required to avoid slew-rate limiting at full output from 20Hz–20kHz.

This is an interesting proposition. You can determine Q_3 collector current using the $Q_4D_8D_9R_{10}R_{11}$ current source and the quiescent M_1 drain current will, ignoring Q_3 base current, be $1.4V/R_8 - I_{CQ-Q3}$, i.e., M_1 quiescent drain current is set by the value of R_8. The servo-controlled first-stage active load takes care of the rest, producing both the desired second-stage bias currents and near-zero quiescent output voltage. What a bargain!

There is some loss of signal current in R_8, a loss that could be eliminated with a current source. Little difference in performance was seen on the breadboard. Anyway, as long as the impedance "looking" into the emitter of Q_3 is significantly less than the value of R_8, the signal current loss is inconsequential. Obviously, a resistor is cheaper and occupies less board space than a constant-current source.

Without the use of active loads for Q_1 and Q_3, the preamplifier could not meet the low-frequency open-loop gain requirement, $a(jf) >$ 100dB. Of course, the advantage of an active load is lost unless impedance at the output node is high, i.e., provided the input impedance of the following stage is high. At the output of the first stage, impedance remains high due to the high impedance "looking" into the M_1 gate. The second stage must drive the input impedance of a control preamplifier or perhaps a potentiometer. Such an impedance is typically tens of kilohms at a minimum.

To be sure this design met reasonable interface requirements, testing was done driving a 10kΩ resistor. Voltage sampling at the output reduces output resistance by the factor $1 + \beta a$. The net effect is that little fall in output voltage is seen over the audio band when the output is shunted by 10kΩ, indicating that output resistance is significantly less than this.

For those who think they hear degradation in sound reproduction due to active loads, I would say that the alternative is added gain stages, which no one likes. In addition to setting current-source current, R_{10} raises the Norton-equivalent resistance "looking" into the collector of Q_4. This latter effect potentially boosts gain because no-load second-stage gain is approximately $-g_{m-M1}R_{Norton}$.

Next month, in the final part of this series, we'll examine power-supply considerations. *aX*

* S = Siemens, new name for mu (μ).

REFERENCES

19. Horowitz and Hill, *op. cit.*, p. 460.

20. Nelson Pass, "DIY Op Amps," Part 2, *Audio Electronics* 1/99, p. 31.

21. Horowitz and Hill, *op. cit.*, p. 432.

22. Brian Clark, "DC Servo Loop Design for Audio Amplifiers," *TAA* 3/82, pp. 14–23.

23. *Discrete Semiconductor Products Data Book*, National Semiconductor Corp., 1989 Edition, pg. 1–30.

24. Mr. Brad Wood, personal correspondence.

PARTS LIST

Parts are specified for one channel only, except as noted.

PREAMPLIFIER

Resistors are 1%, metal film, 0.25W resistors unless otherwise specified. Values are in ohms.

R_{in} – See text
R_{iso} – 10.0
R_1 – 49.9K
R_2 – 4.02K
R_3 – 5.00 (two paralleled 10Ω resistors)
R_4,R_9,R_{11} – 4.99K
R_5 – 392
R_6 – 600
R_7 – 1.00K
R_8 – 15.0, 1W
R_{10} – 18.2
R_{12} – 1.00M
R_{13} – 20K

Capacitors are 2%, 50V polypropylene film capacitors unless otherwise specified. Values are in farads.

C_{rf} – 10n, 100V ceramic disc
C_1 – 56n
C_2 – 20n (formed by paralleling two 10nF capacitors)
C_3 – 1μ
C_4 – 390p
C_5,C_6 – 100n, 25V ceramic disc

Diodes

D_1–D_9 are 1N4148 silicon signal diodes.

Transistors

J_{1A}–J_{1D} – 2SK170 JFETs
M_1 – IRF511 MOSFET
Q_1 – BC549C BJT
Q_2 – BC559C BJT
Q_3 – TIP30C BJT
Q_4 – TIP29C BJT

ICs

U_1 – LF411A